Towards a two-qubit spin quantum computing architecture in Silicon

PH 591 : Dual Degree Project 2

by

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Declaration

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Abstract

With the advent of better technologies, measurement and control of spin qubits is no more a dream. Spin qubits have taken the fields of quantum technology, quantum computing to a new height. Electrons confined in solid-state systems show great promise for quantum applications. This thesis talks about our effort towards the fabrication of double quantum dot architecture on Si/SiGe heterostructure. The fabrication effort comprises optimization of the various process for the tools available at IIT Bombay. This thesis also discusses our fabrication effort of building hall bars on the Si/SiGe heterostructure to observe 2D physics. A part of our latest ongoing work on using numerical tools for simulating architectures is also included.

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Chapter 1

Introduction

In the past decade, there has been tremendous progress in the experimental development of a quantum computer: a machine that would exploit the full complexity of a many-particle quantum wavefunction to solve a computational problem. People have shown endless applications of quantum mechanics. The famous ones being using quantum computers for quantum simulations as proposed by Feynman[3], exponential speedup for factorization of large number[6] and polynomial speedup in searching database[4].

The fundamental essence of a quantum computer is its qubits. The qubit is a quantum mechanical bit with two states $|0\rangle$ and $|1\rangle$. The qubit can be in a complex superposition of these two states, unlike any classical bit.

There is a wide range of physical systems in which qubits can be implemented. Researchers have shown qubit implementation using trapped ion, a solid-state system including semiconductors, superconductors. New systems like Nitrogen-Vacancy Centers, topological insulators, Majorana fermions have peaked interests of many.

The primary challenges for creating a quantum computer are called DiVincenzo Criteria which are as follows [2]

1. A robust and scalable physical system with well-characterized qubits.
2. The ability to initialize the state of the qubits to simple fiducial state, such as to $|000 \cdots 000\rangle$
3. A "universal" set of quantum gates.
4. Long relevant decoherence times, much longer than the gate operation time.
5. A qubit-specific measurement capability.
6. The ability to convert stationary qubits to flying qubits.

7. THe ability to successfully transmit the flying qubits between specified locations.

In this project, we take on the challenge of creating qubits using quantum dots in Si-SiGe Heterostructures.

1.1 Report Outline

The second chapter is a brief discussion on the theory on how to realize a quantum computing architecture using the electron spin within a Si-SiGe based heterostructure. The next chapter talks about the CAD designs and the fabrication process for a double quantum dot and hall bar. From the fourth chapter until the sixth chapter, the fabrication related work is described. The fourth chapter is about the progress on the fabrication of the double quantum dot architecture. The fifth chapter is about the various optimization process carried out. The sixth chapter is about the progress on fabrication of the hall bar architecture. The seventh chapter is about the numerical results of simulating a double quantum dot architecture.

Chapter 2

Realizing spin qubit architecture in silicon

There are multiple layers of abstraction of physical concepts required to understand the possibility of realizing quantum architecture in silicon. Each layer is rich with its subtlety. Here, in a brief manner a top-down breakdown of the layers will be done i.e. going from mathematically defining qubit to the two dimensional electron gas theory to trap a single electron.

2.1 Quantum analog of a classical computer

Classical bit to quantum bit

The essential component of any classical computer is the definition of information which is a bit. A bit can either be "1" or "0" and physically it is realized by creating a "two-level system (TLS)". The TLS basically corresponds to the state of any device in the computer like MOSFET (metal oxide-semiconductor field effect transistor) when "high" and "low" voltage is applied the gate terminal.

To jump over to quantum analog, the TLS chosen is way more fundamental like the two spin states of a spin - 1/2 system (up-spin and down-spin) or the two polarisation states of the photon (ex. verical and horizontal polarisation) or the quantized flux in a supercoducting circuit. These states define the "0" and "1" of the quantum architecture. One trivial obvious benefit is that the whole circuitry can be made denser.

Superposition and what it implies

However the benefit of the quantum architecture comes into play because of the quantum-only behaviour of superposition. Superposition implies that the quantum-TLS can not only be just states “1” and “0” but also in any one of the infinite possible linear superposition of these states. The quantum bit (a.k.a. qubit) is mathematically represented as

$$|\psi\rangle = \alpha_0 |0\rangle + \alpha_1 |1\rangle \tag{2.1}$$

where, the complex numbers α_0 and α_1 are known as the probability amplitudes, such that $|\alpha_0|^2$ and $|\alpha_1|^2$ represent the probabilities of finding the qubit in the ”pure” state $|0\rangle$ and $|1\rangle$ repectively. Thus,

$$|\alpha_0|^2 + |\alpha_1|^2 = 1 \tag{2.2}$$

Without loss of generality and some basic algebra the state can be written as follows

$$|\psi\rangle = cos(\theta/2) |0\rangle + e^{i\phi} sin(\theta/2) |1\rangle \tag{2.3}$$

where, $\alpha_0 = cos(\theta/2)$ and $\alpha_1 = e^{i*\phi} sin(\theta/2)$. This representation helps in geometrical representation of the qubit on the surface of a unit sphere, where each position is defined by (θ, ϕ). This sphere is called the bloch sphere.

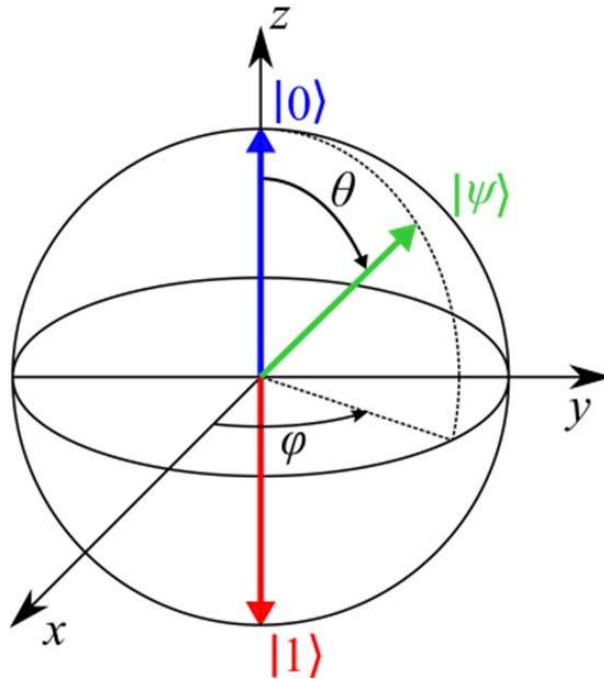


Figure 2.1: The geometrical representation of the Hilbert space spanned by the qubit

The north and south poles of the bloch sphere represent the "pure" state $|0\rangle$ and $|1\rangle$ repectively. All other locations are some superposition of these pure states. Thus a single qubit can store "0" and "1" simultaneously. Thus "N" qubits will store equivalent of 2^N bit data. However while retrieving this data is probabilistic and only one of these 2^N possible states will be measured.

Effect of measurement in quantum computer

To intelligently retrieve a state which is required is where quantum algorithms come into picture. This state can be the solution of some problem or can be just some data which is to be retrieved. Quantum algorithms is all about manipulating states such that probabilities start getting accumulated in the state which is desired.

Amongst all other possibilites of choosing a particular system for the basic building block - "qubit", we choose the spin of the electron.

2.2 Creating Spin Qubit

As mentioned earlier the up and down spin states of the electron are chosen as "1" and "0" respectively. However in the natural scenario, energetically both these states are degenerate. Hence the first task is to break the degeneracy

Breaking the degeneracy

By applying a strong static magnetic field the spin which has a magnetic moment interacts with the field to break the degeneracy. The Hamiltonian is given as $H = -\frac{\mu_B g_s}{\hbar}\vec{S}.\vec{B}$ where μ_B is the bohr magneton, g_s is the Lande g-factor for electronic spins. The eigen-energies are $\pm\mu_B g_s B_0$. This system will from now be referred as a spin qubit.

Fidelity of the qubit

Now that theoretically the system has been defined before moving on to the experimental procedure, an important checklist to complete is the Di-Vincenzo criterion.

To check spin-qubit robustness, the T_2 value (time taken for spin to get dephased i.e. decoherence time scale) is compared to the timescale of the gate operations. Higher the T_2 and lower the gate operations better would be the robustness. The T_2 for silicon spin-qubits have been measured as high as 600 millisecond, while gate operations can be performed within ten to hundred nanoseconds. The essential reason for a high T_2 for silicon spin-qubits is the lack of nuclear spins in the environment of

the more-abundant ^{28}Si(96%) isotope and weak spin-orbit coupling. The T2 will keep on improving as the quality of silicon manufactured keeps on increasing.

The other criterion is scalability, which has been the sore point for many other quantum systems. However for silicon spin-qubit, the QC - architecture depends on elements and techniques already well-established for the traditional micro-electronics industry. Hence there is no need to reinvent the wheel for silicon spin-qubits.

Isolating single electrons

To get a spin, one needs to isolate and trap a single electron. A quantum dot based architecture is used to isolate a single electron. A standard desgin is displayed in the below.

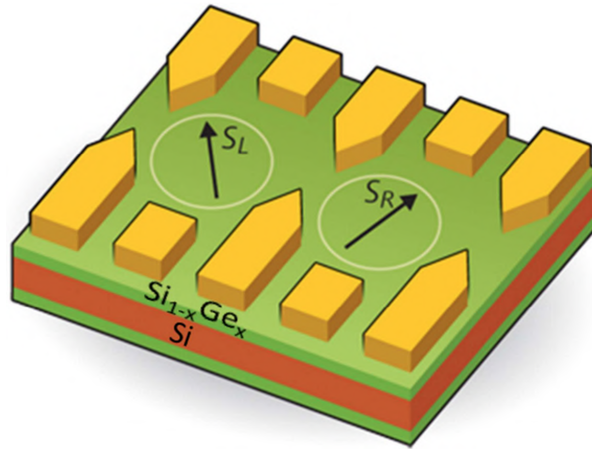


Figure 2.2: Standard spin-qubit design showing two tunnel-coupled single electron quantum dots, electrostatically induced in a buried 2d electron gas formed at the interface of a Si and $Si_{1-x}Ge_x$ epilayer. *(Courtesy : Joint Quantum Institute)*

The quantum dots are defined electrostatically by surface gates (arrow-like shapes in yellow) acting like barriers and trapping the electron located in the 2d electron gas layer formed because of sandwiching Si (orange) between $Si_{1-x}Ge_x$ (green) layers. The quantum dots are tunnel-coupled with each other while capacitively coupled to the plunger gates which control the electrochemical potential of the QDs.

2.3 Single Qubit Gates

The first step towards a universal gate structure are single qubit gates. The method to apply single spin-qubit gates is independent of the system and has been borrowed from the first field to do it i.e. NMR.

Geometrical implication of Single Qubit Gates

On the bloch sphere, a single qubit gate is simply a rotation. For example the gate X is simply a 180 rotation along the X axis. The Hadamard gate for example is equivalent to rotation of 180 along the Z-axis followed by 90 rotation along the Y-axis. Thus all single qubit gates can be broken down to rotations about any two axis.

Electron Spin Resonance

To apply these rotation ESR is used in which a bursts of radio frequency signal in resonance with the Zeeman splitting is sent to the spin. The spin qubit interacts with the magnetic field of the RF signal which causes an effective rotation of the spin qubit in a rotating frame. This rotating frame is rotating along the Z-axis (along which the static magnetic field is applied) with frequency equal to the RF's frequency i.e. the zeeman splitting frequency. Thus by controlling the duration and the phase of the pulse one can realize the spin-rotations along the x- and y-axes.

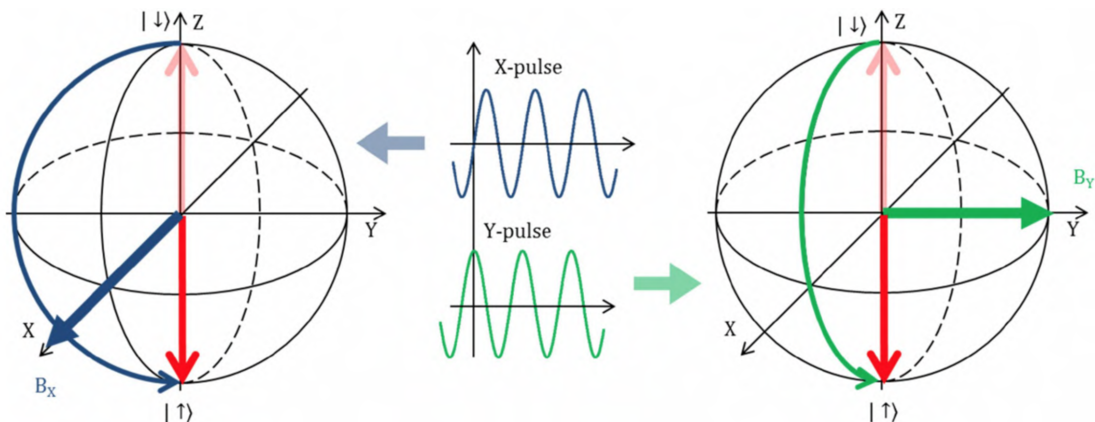


Figure 2.3: Rotations generated by RF pulses based on the Electron spin resonance phenomenon.

For a $B_0 = 1T$, the Zeeman splitting (in silicon) is $118\mu eV$. The resonance condition in ESR is then acheived for a RF frequency of $27.998GHz$. The strength of the RF signal (Rabi Frequency) dictates the time taken for the gate to be applied. Typically ESR gated can operate at a few MHz.

2.4 Two Qubit Gates

Types of two qubit gates

Universal quantum computing architecture requires at least one two qubit gate along with the the one qubit gate set. Such two qubit gates which complete the universality are generally of the type C-U gate. The C-U operator has one control qubit when "1" the U gate is applied to the other qubit and when "0" nothing is done to the other qubit. The simplest example is the CNOT gate which operates as follows,

$$U_{CNOT}\left|\Psi_{in}\right\rangle = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \alpha_{\downarrow\downarrow} \\ \alpha_{\downarrow\uparrow} \\ \alpha_{\uparrow\downarrow} \\ \alpha_{\uparrow\uparrow} \end{bmatrix} = \begin{bmatrix} \alpha_{\downarrow\downarrow} \\ \alpha_{\downarrow\uparrow} \\ \alpha_{\uparrow\uparrow} \\ \alpha_{\uparrow\downarrow} \end{bmatrix} = \left|\Psi_{out}\right\rangle \tag{2.4}$$

In Spin QC architecture the two qubit gate that can be built easily is the SWAP gate. As the name suggest, SWAP gate swaps both the spins shown as follows,

$$U_{SWAP}\left|\Psi_{in}\right\rangle = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \alpha_{\downarrow\downarrow} \\ \alpha_{\downarrow\uparrow} \\ \alpha_{\uparrow\downarrow} \\ \alpha_{\uparrow\uparrow} \end{bmatrix} = \begin{bmatrix} \alpha_{\downarrow\downarrow} \\ \alpha_{\uparrow\downarrow} \\ \alpha_{\uparrow\downarrow} \\ \alpha_{\uparrow\uparrow} \end{bmatrix} = \left|\Psi_{out}\right\rangle \tag{2.5}$$

Heisenberg Exchange Interaction

To realize the SWAP Gate the interaction between the two quantum dots described as the Heisenberg exchange interaction is engineered. The Heisenberg exchange interaction is given as

$$H_{int} = J(\varepsilon)\vec{S_1}\cdot\vec{S_2} = J(\varepsilon)/2\left[\left(\vec{S_1}+\vec{S_2}\right)^2 - \vec{S_1}^2 - \vec{S_2}^2\right] \tag{2.6}$$

Where, ε is the energy detuning between the two single-electron levels in the neighbouring quantum dots. The eigenvectors for this interaction Hamiltonian are the singlet and the triplet states of the two quantum dot.

The energy detuning controlled by the plunger gates determine the coupling between the two single electron levels of the neighbouring QDs and thereby the magnitude of $J(\varepsilon)$.

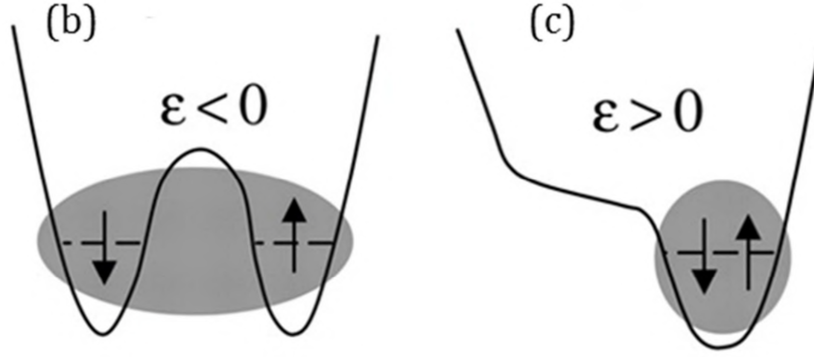


Figure 2.4: (b) The energy landscape along the black dotted line for negative detuning (b) for a positive detuning (*Courtesy: J. Petta et al,*Science 309, 2180 (2005)

In the energy landscape shown in the Figure 2.4, when the detuning is negative one electron is confined in each of the two quantum dots. However when the detuning is positive both the electrons occupy the same quantum dot. Therefore by using the plunger gates (V_L and V_R) both of these state (1,1) and (0,2) can be accessed.

In the new eigenbasis given by the spin singlet and the spin triplet states the energy variation as a function of the detuning is given in Figure 2.5 (a).

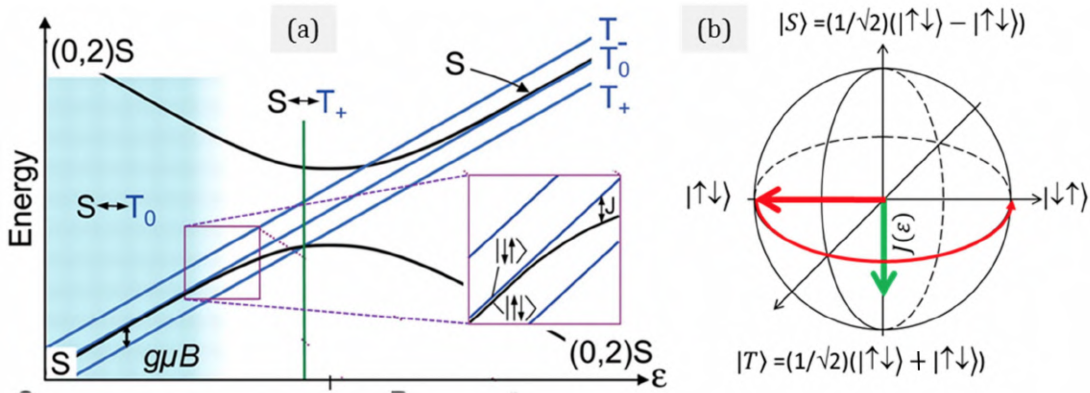


Figure 2.5: (a) The energy variation of the singlet state S, and the three triplet states T_+, T_- and T_0 with the detuning ε. For $\varepsilon < 0$, the charge configuration is (1,1), while for $\varepsilon > 0$, the charge configuration is (0, 2). (b) The Bloch sphere of the $S - T_0$ (sub-space (Courtesy: J. Petta et al, Science 309, 2180 (2005)).

Among the space of single and triplet states, we need to choose only the S and T_0 where the spins are getting flipped around. To do this a magnetic field is applied which will create a Zeeman splitting among the triplet states as shown by the three blue line in Figure 2.5 (a).

Now in this subspace as shown by the bloch sphere in Figure 2.5 (b) the interaction Hamiltonian is along the Z- axis, creating a rotation along the Z-axis. Thus if the initial state is prepared as $|\uparrow\downarrow\rangle$, the interaction will rotate it to the $|\downarrow\uparrow\rangle$ state in time $\frac{\hbar\pi}{J(\varepsilon)}$.

To do this we want quick control on $J(\epsilon)$ and this is only possible when $\epsilon < 0$ as seen in the Figure 2.5 (b). where the $S - T_0$ splitting is small and dependent on detuning. Thus by choosing appropriate detuning the SWAP gate can be prepared

In so far, it has not been described how to initialize the two qubit input in the $|\uparrow\downarrow\rangle$ (or in $|\downarrow\uparrow\rangle$) state. To initialize in these states one needs to have a magnetic field gradient (ΔB_x) between the QDs. In presence of a gradient magnetic field the control Hamiltonian of the two qubit system in the subspace is

$$H = \begin{bmatrix} -J(\varepsilon) & \frac{g\mu_B}{2}\Delta B_x \\ \frac{g\mu_B}{2}\Delta B_x & 0 \end{bmatrix} \tag{2.7}$$

for sufficently negative detuning ε, if the condition $-J(\epsilon) \leq g\mu_B \Delta B_x$ can be realized then the two-qubit input is initialized in the $|\uparrow\downarrow\rangle$ or in $|\downarrow\uparrow\rangle$ state.

2.5 Spin Detection

There are two methods for spin detection. Both of them will be discussed briefly

Spin-to-charge conversion and charge sensing

One method is to effectively convert spin to charge and then measure the charge. Let's begin with charge sensing. This is done using Single Electron Transistors (SETs) or Quantum Point Contact (QPC). A layout of SET coupled to QD is shown in Figure 2.6 (a). The qubit (D_2) is both capacitively- and tunnel-coupled to a SET defined by the source (S) and drain (D) terminal, a large island (D_1) and a plunger gate (G_1). Voltages on the gate G_1 (V_{G1}) and the qubit plunger gate G_2 (V_{G2}) control the electrochemical potential of both the SET-island (D_1) and the qubit (D_2).

With a small source drain (V_{SD}) bias between the source and drain of the SET, sweeping V_{G1} alone yields a series of current peaks due to the coulomb blockade effect explained in the previous BTP report. When both V_{G1} and V_{G2} are swept, the current peaks appear as inclined lines as shown in the $V_{G1} - V_{G2}$ map in Figure 2.6 (b).

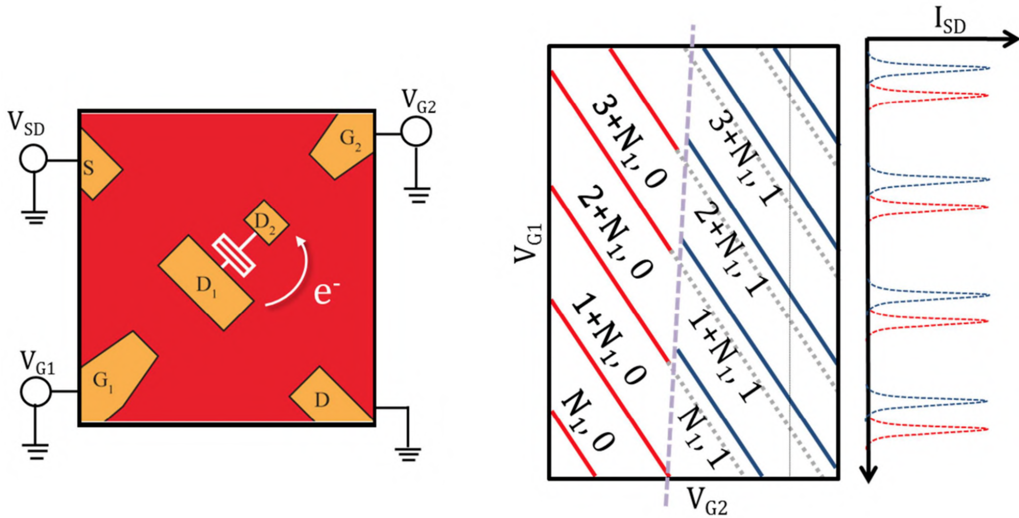


Figure 2.6: (a) Schematic layout of charge sensing with a SET, which is both capacitively- and tunnel-coupled to the qubit (b) The current map of the SET-island. Along the purple line, charge transfer takes place between D_1 and D_2, and in response the bias point of the SET shifts. This enables sensing of the qubit charge state (Courtesy: S. Mahapatra et al., Nano Lett. 11, 4376 (2011))

Across these lines, a transfer of electron between the SET and the quantum dot takes place depending on how V_{G1} and V_{G2} is varied. At the line the electrochemical potenctial matches and the transfer happends. Moving from left to right of this line (increasing V_{G2}) an electron is transfered from the SET to QD. Due to the capacitive coupling between D_1 and D_2, the decrease in the charge number on the SET shifts the bias point and thus the current lines are shifted from red to blue. This shift in the peak thus allows us to sense the charge state of the qubit non-invasively.

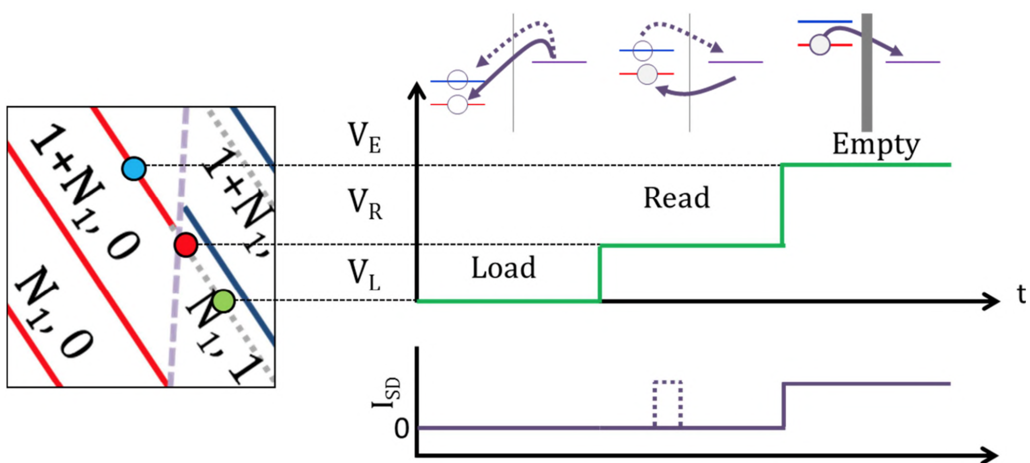


Figure 2.7: Single-shot projective spin read-out by spin-to-charge conversion and charge sensing.

In the presence of the static magnetic field, appropriate control of V_{G1} and V_{G2} enables spin readout. The scheme is shown in Figure 2.7. At the read point, both the D_1 and D_2 have equal electrochemical potential. However the trick is using static magnetic field which splits the states into two different energy level. The spin-down level which is slighly higher can transfer electron to the SET but the spin-up level cannot transfer electron to the SET. This disparity is the heart of spin sensing.

Pauli spin blockade and charge sensing

Instead of depending on the spin-to-charge conversion, one may make use of the Pauli spin blockade phenomenon, which however involves an ancillary single-electron QD. To understand this technique consider the situation where the QD and the ancillary QD both have one spins. When the detuning $\varepsilon \ll 0$ the interaction between the QD is negligeble and the QD can be manipulated independently. Now to measure the detuning is increased in a pulsed manner. The trick over here is that $S - T_0$ splitting is very large in (0,2) configuration. Hence if the two spin state is initially singlet S(1,1) then transition to S(0,2) is allowed however if the initial state is triple T(1,1) then the transition to T(0,2) is blocked. This phenomenon is called spin blockade and can be used to non-invasively measure the spin states.

Chapter 3

Device Design and Fabrication

The following chapter has been covered extensively in the previous BTP Report. This a brief chapter on the designs of the device. The fabrication steps have been updated after lot of deliberation and have been written down explicitly.

3.1 Quantum Dots Design

The design has two quantum dots sitting beside each other with multiple accumulation gates and depletion gates to define the shape and controlling the charge each quantum dot has and interaction among themselves. In the complete CAD Design, like any device the pink squares are the bonding pads and several connection lines flow from them to the devices inside

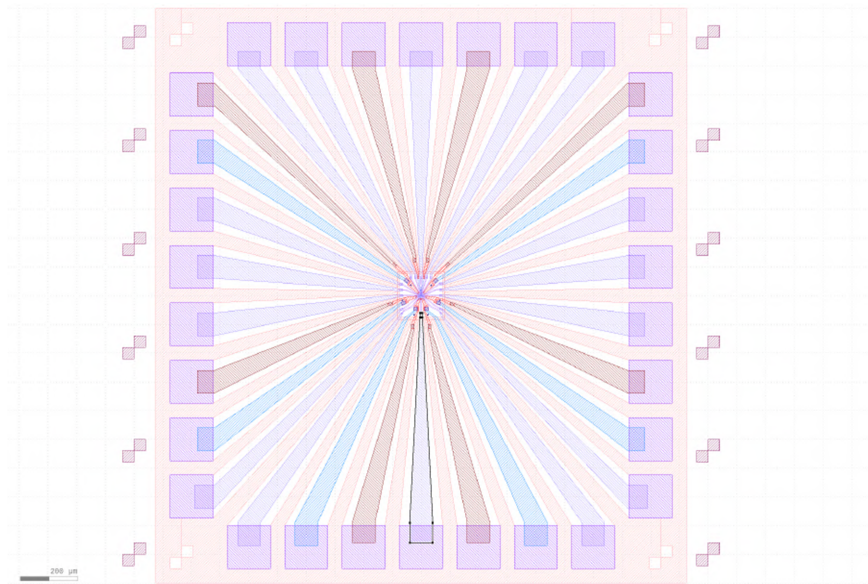


Figure 3.1: Complete CAD design

The two dots are located in the central part as shown. The blue structure are the accumulation gates and the pink are the depletion gate. In the two images below all the different parts have been labelled up. Transfer point is a place where in the lithography process the write field is changed. So at transfer point the fine designs from the centre of the pattern meet the bigger designs from the outer part of the pattern.

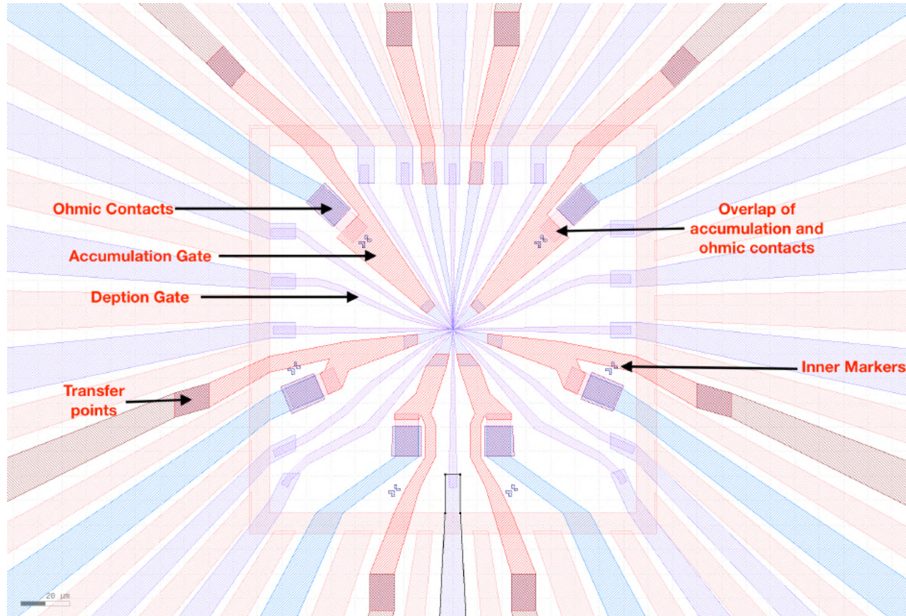


Figure 3.2: CAD design of the mesa structure

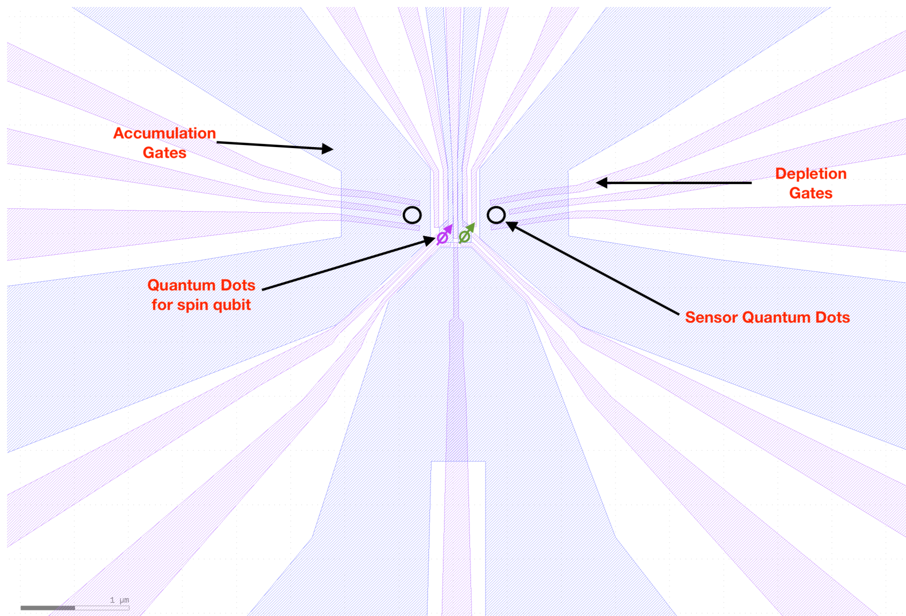


Figure 3.3: CAD design of the two quantum dots

3.2 Quantum Dots Fabrication

After a lot of deliberations and discussion, the following is the final step-by-step procedure.

Sr No	Process Name	Purpose
1	Cut Sample	Cut Sample in 1cm by 1cm pieces
2	RCA Cleaning	Standard Cleaning procedure.
3	Atomic Layer Deposition	Create a base layer of Al_2O_3
4	Electron Beam Lithography	Make design pattern of inner markers and outer markers
5	Metallization	Metal Deposition in the pattern (Pt Al)
6	Electron Beam Lithography	Make design pattern for the mesa structure
7	HF Dip	Remove out aluminium oxide from the patterns exposed
8	Etching	Etch out the regions patterned to create the mesa structure
9	Atomic Layer Deposition	Deposit uniformly aluminium oxide all over the sample
10	Electron Beam Lithography	Write Pattern for phosphorous ion deposition
11	HF Dip	Remove out aluminium oxide from the patterns exposed
12	Phosphorus Ion Deposition	Phosphorous ion deposition
13	Electron Beam Lithography	Write Pattern for phosphorous ion deposition
14	Metallization	Metal Deposition in the pattern (Ti Al)
15	Annealing	Annealing to complete ion deposition
16	Electron Beam Lithography	Make design pattern for fine and large depletion gates
17	Metallization	Metal Deposition in the pattern (Pt Al)
18	Electron Beam Lithography	Make design pattern for connector lines
19	Metallization	Metal Deposition in the pattern (Pt Al)
20	Atomic Layer Deposition	Create a layer of Al_2O_3
21	Electron Beam Lithography	Creating patterns at the overlapped parts
22	HF Dip	Etch through Al_2O_3 at the overlapped parts
23	Electron Beam Lithography	Accumulation Gates
24	Metallization	Metal Deposition in the pattern (Pt Al)

Table 3.1: Step by step procedure for fabricating double quantum dot

3.3 Hall Bar Design

The hall bar design is taken from the TU Delft group. The first hall-bar (left one) is of the size $40\mu m$ by $310\mu m$. The second hall-bar (right one) is of the size $50\mu m$ by $160\mu m$.

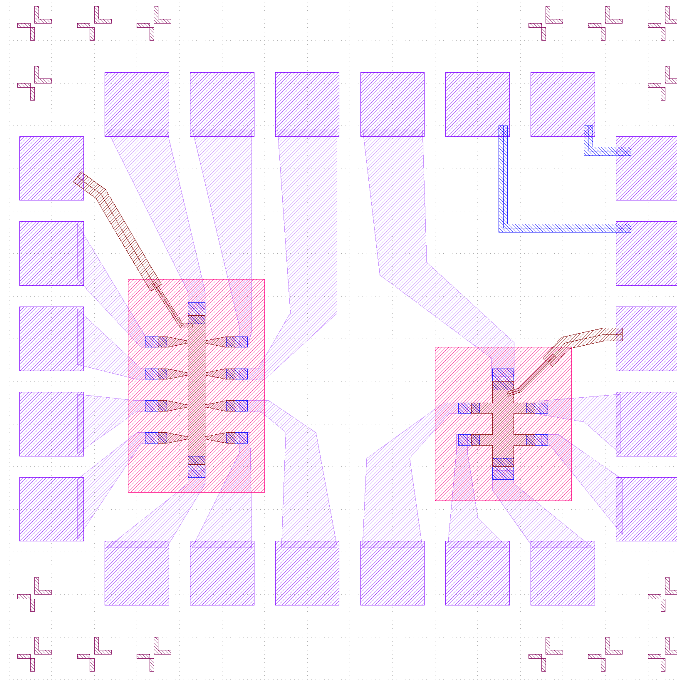


Figure 3.4: 2D CAD design of Hall Bar

The yellow are the accumulation gates which will attract the electron gas beneath it. The purple connections to the top and the bottom of the hall-bars will be for controlling the current flowing through the sample or the voltage. The side purple connectors are for measuring the transverse voltage on the hall bars. Both of these connectors (side and top-bottom) have to be in ohmic contact with the 2DEG.

However only the left hallbar is the one which is being made currently because the other space is being used for making devices for Shobhna's experiments.

3.4 Hall Bar Fabrication

The procedure has been updated with lot of changes with respect to the last one.

Sr. No	Process	Purpose
1.	Atomic Layer Deposition	Create a Layer of Al_2O_3
2.	Electron Beam Lithography	Make the design pattern for markers
3.	Metal Deposition	Fill the pattern with metal (Pt Al)
4.	Electron Beam Lithography	Make the design pattern for ion implantation windows
5.	Ion Implantation	Implant phosphorous ions at least up to the 2DEG
6.	Metal Deposition	Fill the pattern with metal (Pt Al)
7.	Annealing	Convert phosphorous ions to dopants
8.	Electron Beam Lithography	Make design pattern for connection lines for ohmics and conding pads
9.	Metal Deposition	Fill the pattern with metal (Pt Al)
.	Atomic Layer Deposition	Create a Layer of Al_2O_3
10.	Electron Beam Lithography	Make design pattern for making holes at bond pads
11,	Oxide Etch	Etching out Al_2O_3
12.	Electron Beam Lithography	Make design pattern for accumulation gates
13.	Metal Deposition	Fill the pattern with metal (Ti Al)

Table 3.2: Step by step procedure for fabricating hall bar.

Chapter 4

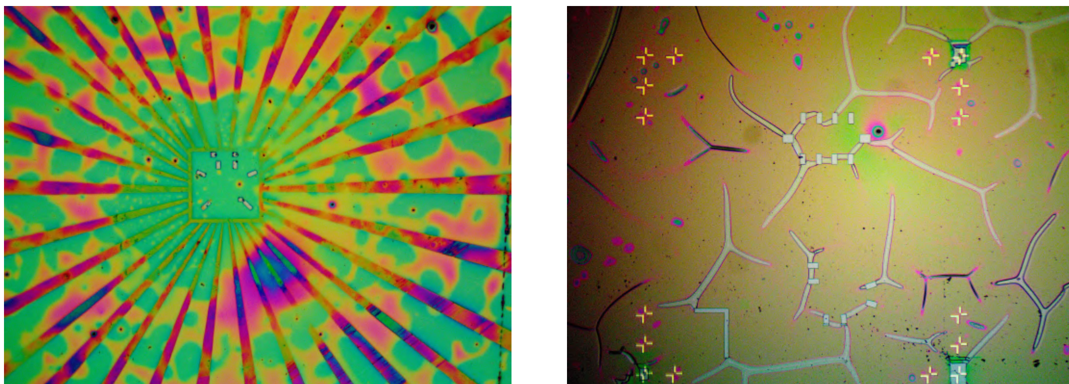
Fabrication : Double QD

4.1 Recap of BTP 1 and 2

BTP 1 and 2 comprised optimisation of the following steps as given in Table 3.1

- (Step 1,2,3) Al_2O_3 deposition using the ALD system (Already optimised).
- (Step 4,5) Creating inner and outer markers which comprises of Raith EBL and Sputter Orion.
- (Step 6,8) Creating mesa structure to isolate the double quantum dot which comprises STSRIE and Raith EBL
- (Step 9) Al_2O_3 deposition using the ALD system (Already optimised).

The next step is creating doping at specific locations by (Step 10) writing pattern using EBL, then (Step 11) etching out the oxide layer using HF and followed by PIII (Step 12). While doing HF dip (Step 11) the sample was lost because of the resist getting corroded by HF as shown below



(a) Spots under/in resist : DQD sample (b) Channel on/under PMMA : HBar sample

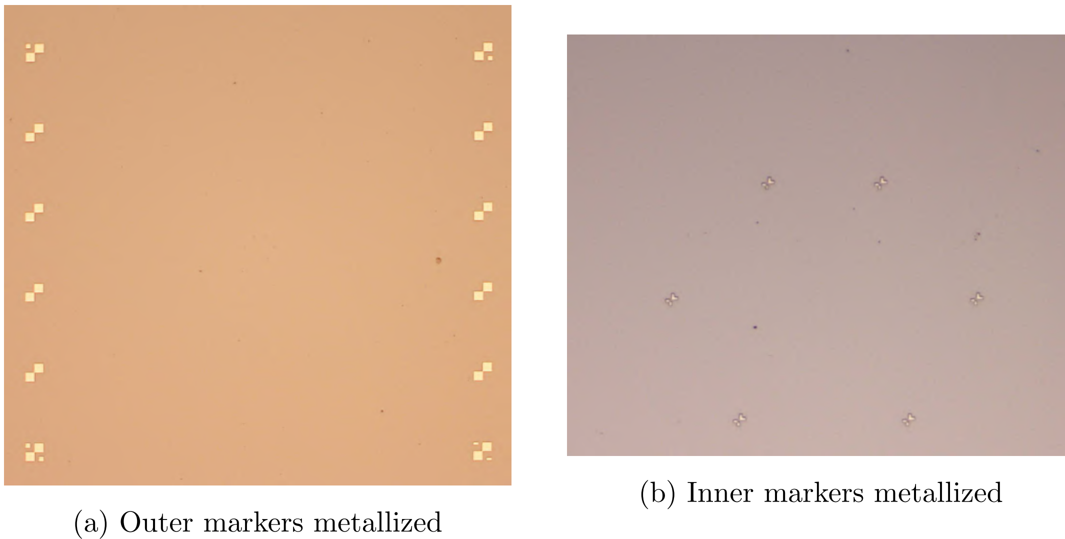
Figure 4.1: Effect of HF on resist

The reason for this will be discussed in the following sections, but the effect of this was that both the samples were destroyed and had to be remade again from scratch.

4.2 Recreating the sample with optimized HF Dip

4.2.1 (Step 1,2,3,4,5) Oxide Deposition and Markers

A pre-ALDed sample was chosen. This step is about creating metal markers of Pt : 30nm and Al : 80nm using Sputter Orion system.



(a) Outer markers metallized

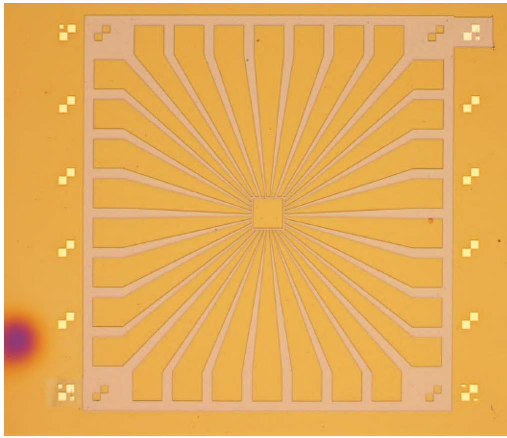
(b) Inner markers metallized

Figure 4.2: Optical microscope images

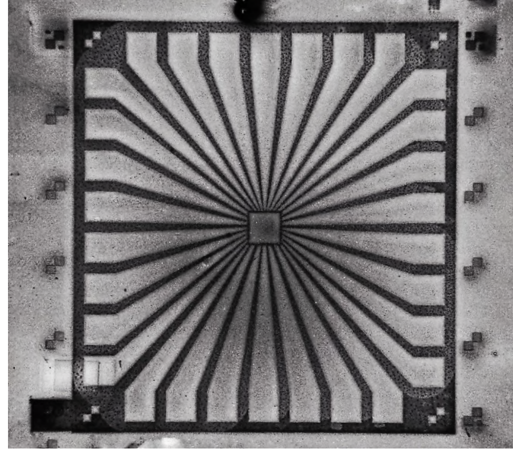
4.2.2 (Step 6,7,8) Etch out Mesa

In this step the HF dip step to remove the Al_2O_3 was optimized. On a side note this step was not done previously because there was no Al_2O_3 layer deposited previously.

To understand the problem thorough SEM and optical imaging of the previous sample were done which showed that the under layer of the resist which was EL9 reacted with HF which led to creation of channels seen previously. Therefore this time only bilayer of PMMA A4 was used. Also rather than using just HF, Buffered HF (7:1) was used since this procedure had worked in another group at TU Delft. These changes effectively solved the problem. This problem turned out to be smaller than imagined. The images are as follows



(a) Optical microscope image after HF dip



(b) SEM image after STSRIE

4.2.3 (Step 9) Oxide layer deposition

Unlike last run, an SEM Image of ALD deposited sample was done which showed the horrible reality of the contamination of samples. Small spot-like structures are seen on the ALD'ed sample surface because of the particles on the surface which hindered the atomic layer deposition to take place. Other reasons need to be verified.

A point to be noted is that these patches are not visible via the optical microscope.

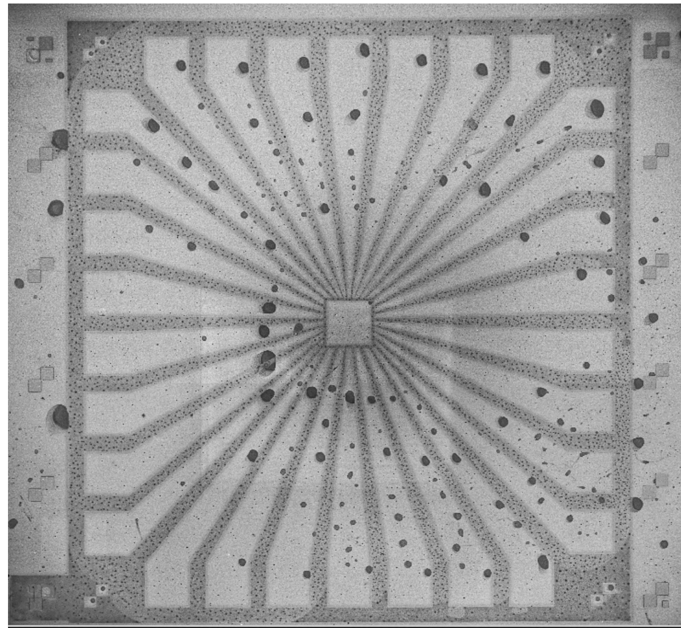


Figure 4.4: SEM image of the post ALD sample showing regions of no oxide deposition

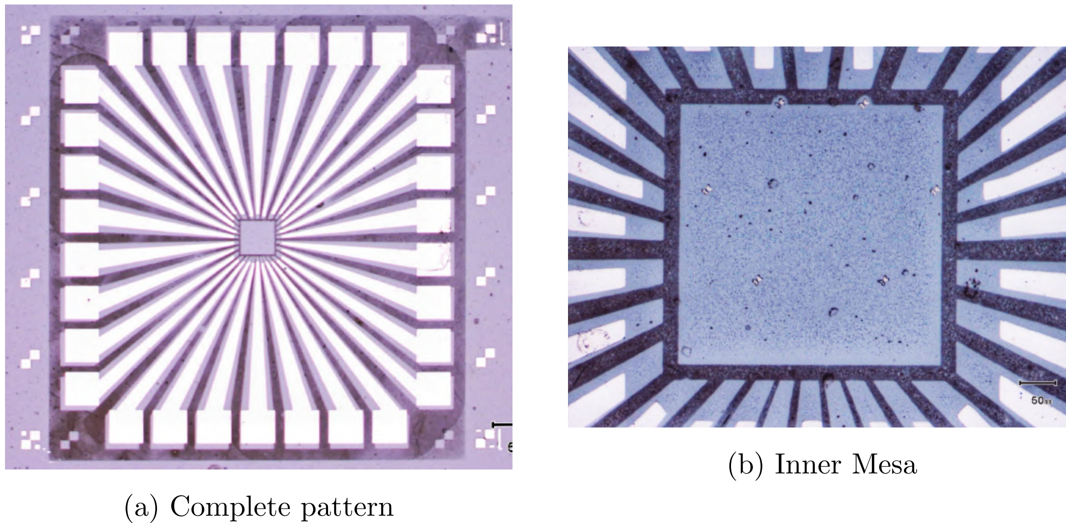
4.2.4 (Step 10,11,12) Phosphorous Ion Implantation

With the optimized HF dip procedure, the oxide etching went perfectly. The phosphorous ion implantation is done with Plasma Immersion Ion-Implantation, which creates a plasma. At this step the problem faced is that the plasma etched the resist and thus the sample was uniformly bombarded with phosphorous ions. This step failed and required series of optimisation.

Since the substrate is silicon and not the the actual heterostructure, the process can be furthered on this sample.

4.2.5 (Step 18,19) Making Bond Pads and connectors

Fine gate step is skipped because it required optimisation and the bond pads step is independent of the fine gate step. The optical images post metal deposition are shown in Figure 4.5



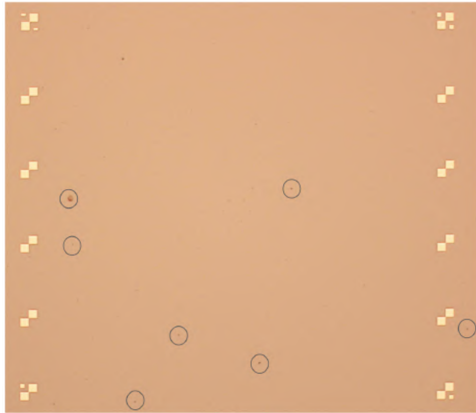
(a) Complete pattern

(b) Inner Mesa

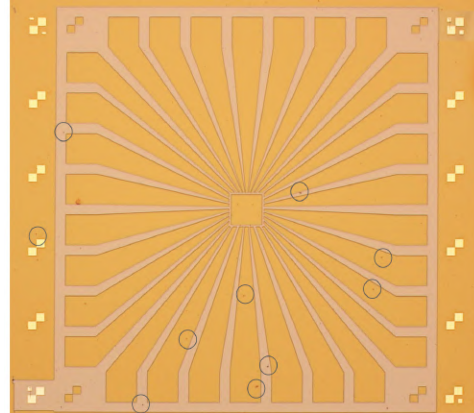
Figure 4.5: Optical Images

4.3 Contamination Prevention Steps

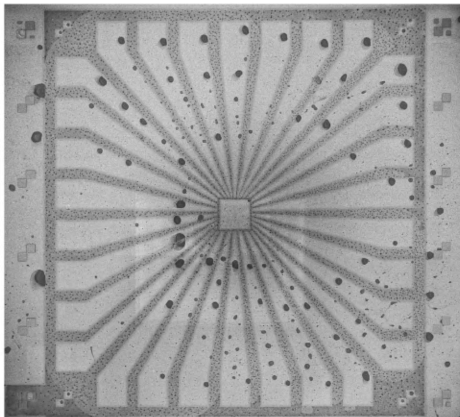
Recalling the steps, the particle count keeps on increasing. The particle keeps increasing due to multiple factors.



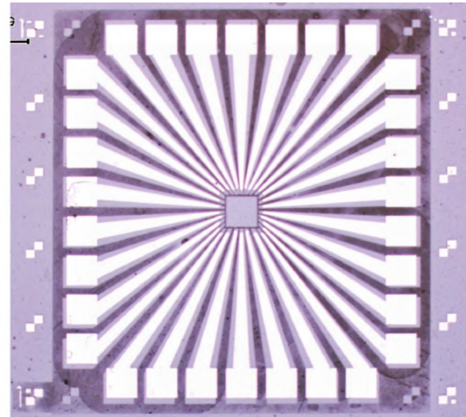
(a) Post Markers



(b) Post Mesa



(a) Post STSRIE



(b) Post Bond Pads and Connectors

The precautions taken from this point (DDP Phase 2) are as follows

1. Acetone and IPA wash after ALD
2. Between RCA cleaning and deposition zero gap in time
3. After diamond scribing acetone sonication and IPA wash
4. Cover sample always with PMMA
5. Oxygen plasma ash before scribing
6. Oxygen plasma ash before PIII
7. Keep samples always inside CEN

Chapter 5

Process Optimisation

5.1 Fine Depletion Gate Optimization

The most significant technological challenge in fabrication of the double quantum dot architecture is patterning the depletion gates with widths of the feature as small as 35nm. Moreover, at a few crucial locations in the design, the separation between two adjacent features is smaller than the neighboring feature sizes. When the separation is smaller than the feature size, the challenge is in patterning and precise metal lift-off. The most challenging piece is where the separation is 27nm, with the adjacent feature size of 35nm.

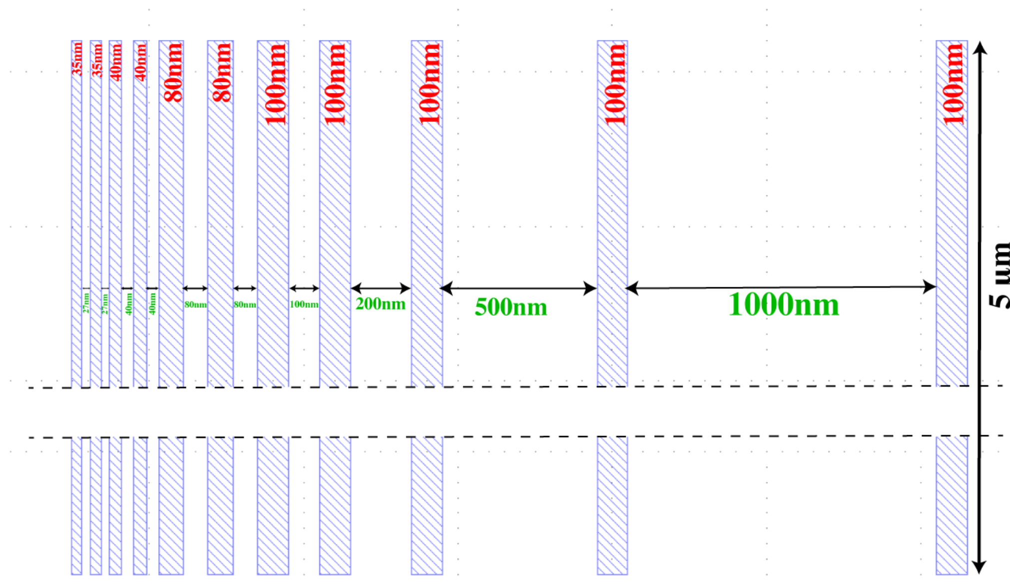


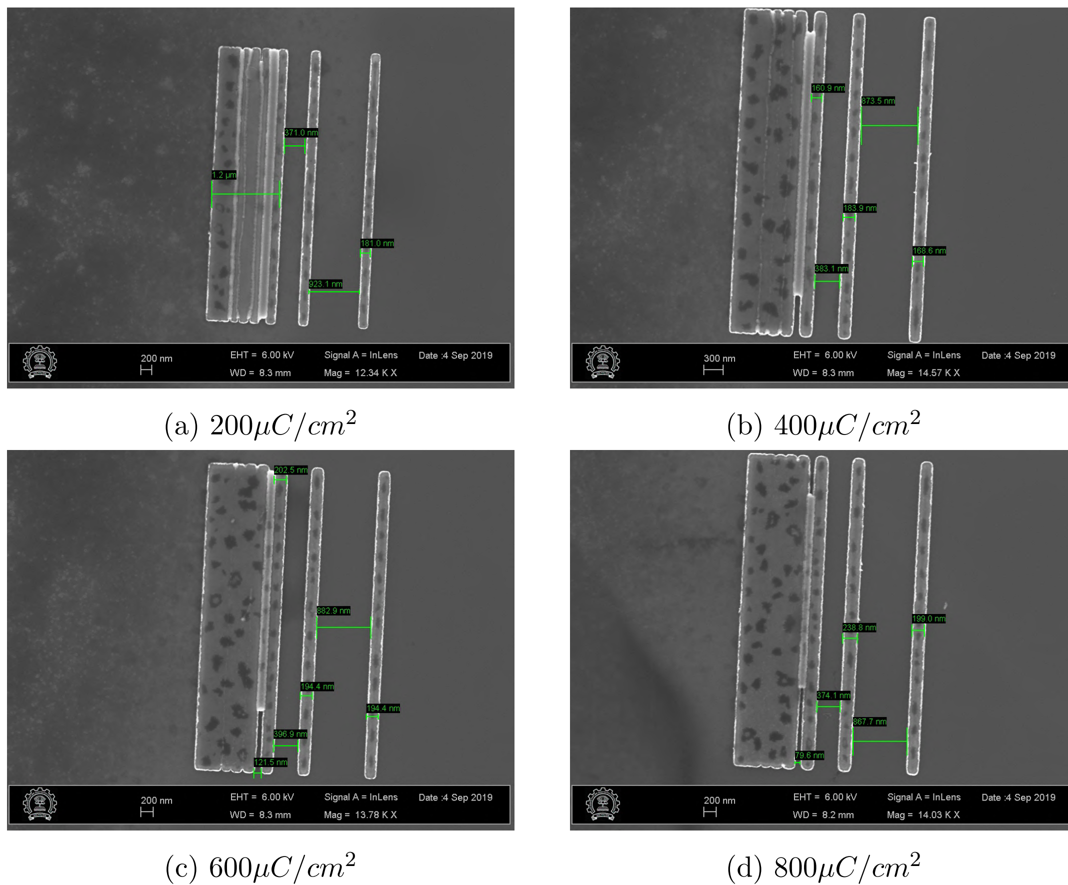
Figure 5.1: CAD file showing the repeating element

For optimization of this lithography step, a pattern file was created (Fig. 5.1), which was a simpler representation of the actual depletion gates. The pattern file's

repeating element contains vertical lines, with varying thickness and varying space between them.

5.1.1 Run 1

The first run was performed at EHT = 20 KV, aperture = $7.5\mu m$ and the resist was a single layer of PMMA A2 950K spun at 4000rpm. The purpose was for optimizing the dosage i.e charge deposited per unit area. The chosen dosages were $200\mu C/cm^2$, $400\mu C/cm^2$, $600\mu C/cm^2$, $800\mu C/cm^2$ and $1000\mu C/cm^2$. The SEM images post metal deposition (Orion Sputter) and lift-off (PG Remover for 6 hours) are shown in Figure 5.2



(a) $200\mu C/cm^2$

(b) $400\mu C/cm^2$

(c) $600\mu C/cm^2$

(d) $800\mu C/cm^2$

Figure 5.2: SEM Images of RUN 1

The patterns, as seen in Fig. 5.2 were bloated, and the reason for this is the high dwell time of the beam. The parameter responsible for the high dwell time is the step size of the beam, which was not correctly set. The other parameter which dictates the dwell time is the dosage, which was approximately in the required range.

5.1.2 Run 2

The second run was carried out at EHT = 25 KV, aperture = $7.5\mu m$, and the resist was a single layer of PMMA A2 950K spun at 4000RPM. The EHT was increased as larger the EHT better the resolution power of the EBL tool. In this run, two parameters were being varied, the step size, which in turn will vary the dwell time, and the dosage. The dwell time is related to the step size of the beam as follows

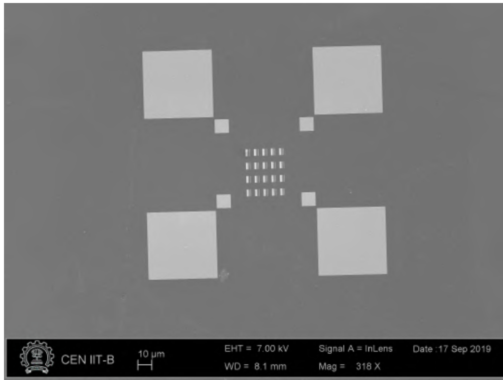
$$T_d = \frac{\delta_s^2 D}{I_B} \tag{5.1}$$

where T_d is the dwell time, δ_S is the step size, D is the dosage and I_B is the beam current. These parameters are related to the beam speed (v_B) as follows,

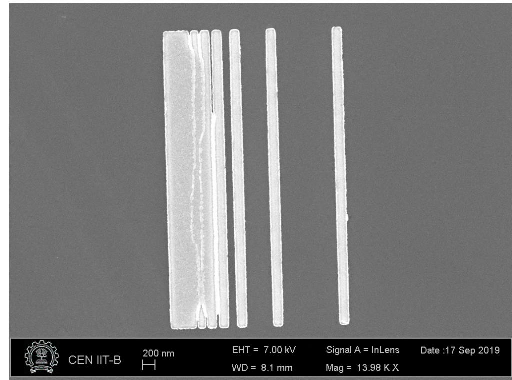
$$v_B = \frac{I_B}{\delta_S * D} \tag{5.2}$$

The dosage variation is from $200\mu C/cm^2$ to $1000\mu C/cm^2$ in 5 steps. A rule of thumb for *RAITH 150-two* is to keep the beam speed between $2mm/s$ to $8mm/s$. Keeping the rule in mind the step size is varied from $1nm$ to $5nm$ in 5 steps. This variation corresponds to the lowest dwell time to higher dwell time. However, as the dosage increases, to keep the beam speed constant, the step size has to decrease. Thus for higher dosages ($> 600\mu C/cm^2$) the beam speed was less than required by the rule of thumb. Hence for these dosages, the dwell time was higher than required but less than what was kept in "Run 1".

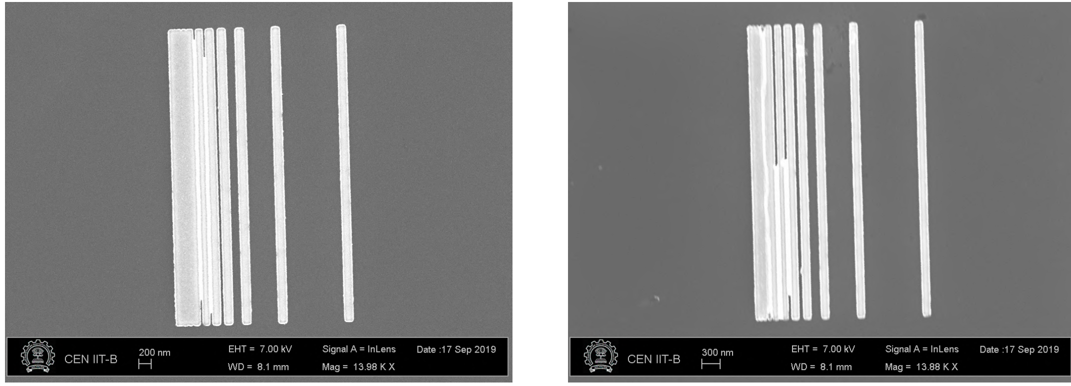
A few of the SEM results obtained post metal deposition (Orion Sputter) and lift-off (PG Remover for 6 hours) are shown in Figure 5.3



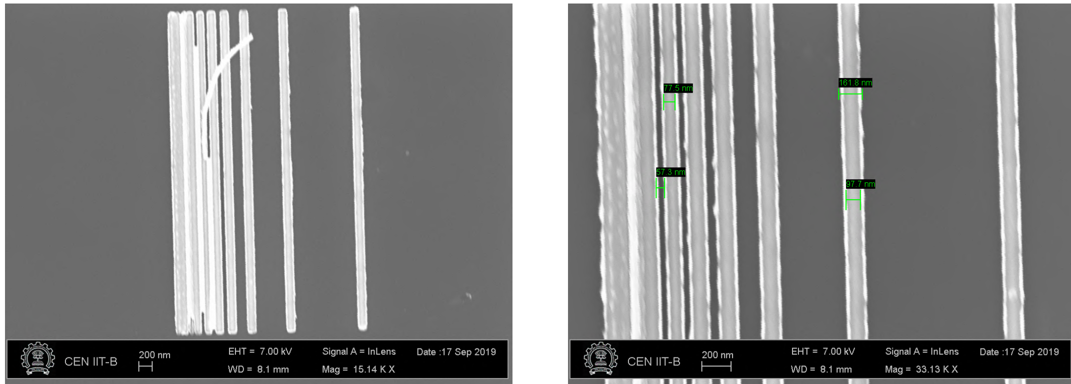
(a) Full matrix of variation



(b) Dosage=$1000\mu C/cm^2$, Step Size = 5nm



(c) Dosage = $800\mu C/cm^2$, Step Size = 1nm (d) Dosage = $400\mu C/cm^2$, Step Size = 4nm



(e) Dosage = $400\mu C/cm^2$, Step Size = 3nm (f) Dosage = $400\mu C/cm^2$, Step Size = 1nm

Figure 5.3: SEM Images of RUN 2

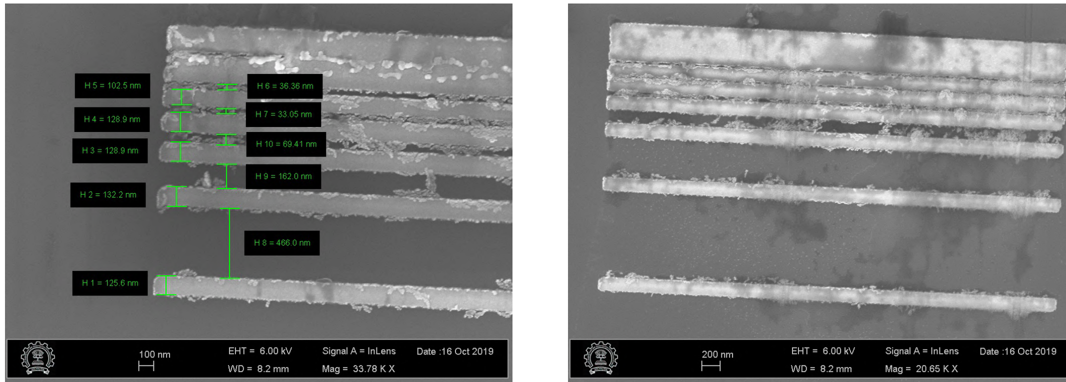
The bright white metal in Fig. 5.3 is part of the metal deposited, which should have been removed during the lift-off. However, the lift-off failed in ejecting out some of the metal, which lead to dangling bright white metal parts. A failed lift-off is probably due to insufficient difference of thickness between the resist and the metal deposited. The resist used was PMMA 950K A2, with a thickness of 80nm. The metal deposited on this was Pt, with a supposed thickness of 30nm. However, on performing profilometry on it, the result obtained was 36-40nm. The increased thickness can be one of the problems for not getting a perfect lift-off. Therefore in the next run, the PMMA thickness will be increased slightly, and the metal deposited will be reduced slightly.

5.1.3 Run 3

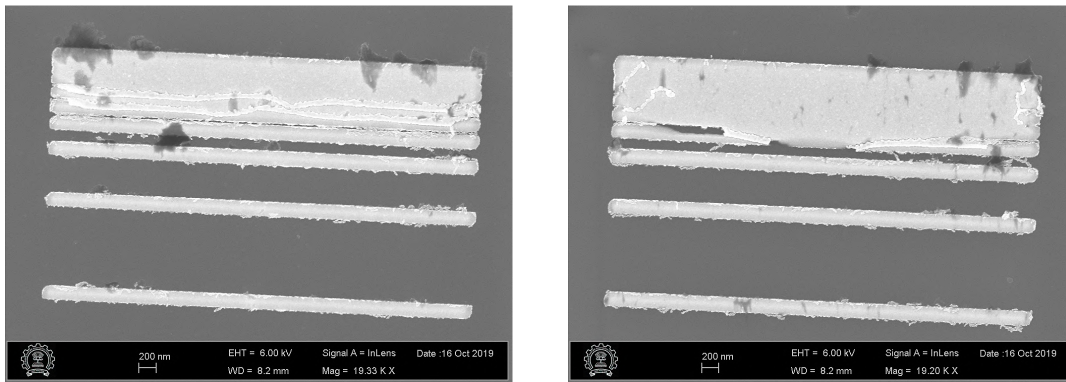
The third run was performed with an EHT = 25KV, aperture = $7.5\mu m$ and the resist was PMMA A2 spun at 3200RPM (instead of 4000RPM as in the previous runs). The variation of the dosage is from $200\mu C/cm^2$ to $1000\mu C/cm^2$ in 5 steps and the step size is varied from $1nm$ to $5nm$ in 5 steps. The thickness of the metal

deposited was reduced to 20nm - 25nm.

A few of the SEM results obtained post metal deposition (Orion Sputter) and lift-off (PG Remover for 6 hours) are shown in Figure 5.4



(a) Dosage = $400\mu C/cm^2$, Step Size = 1nm (b) Dosage = $600\mu C/cm^2$, Step Size = 1nm



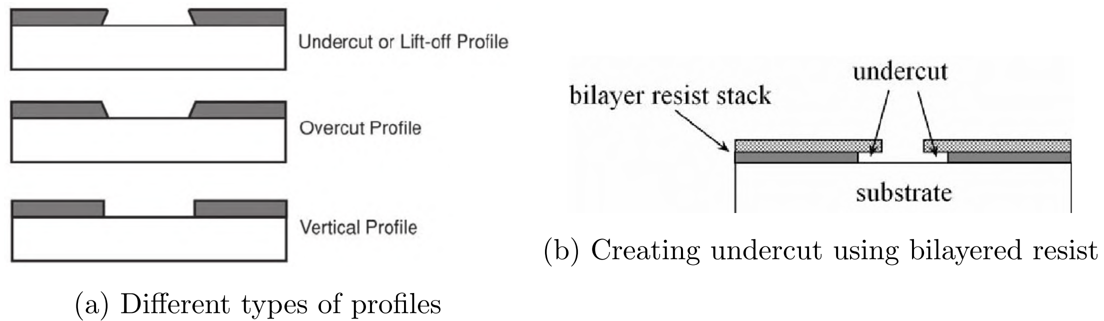
(c) Dosage = $800\mu C/cm^2$, Step Size = 1nm (d) Dosage = $1000\mu C/cm^2$, Step Size = 1nm

Figure 5.4: SEM Images of RUN 3

Minor improvements can be observed in Fig. 5.4, especially for the case of dosage equal to $400\mu C/cm^2$. The excess metal has decreased, and the patterns appear to be thus sharper than the previous runs. However, the patterns are wider than expected by approximately 20nm. For the next run, an offset of -20nm is applied to counteract this effect.

5.1.4 Run 4

A single-layered resist after development gives either a vertical profile or an overcut profile where the resist was exposed to the electron beam. Fig. 5.5a displays the three possible profiles. The best possible profile for precise metallization plus lift-off is the undercut profile. A bilayered resist is required to create an overhang structure to obtain an effective undercut profile, as seen in 5.5b.



(a) Different types of profiles

(b) Creating undercut using bilayered resist

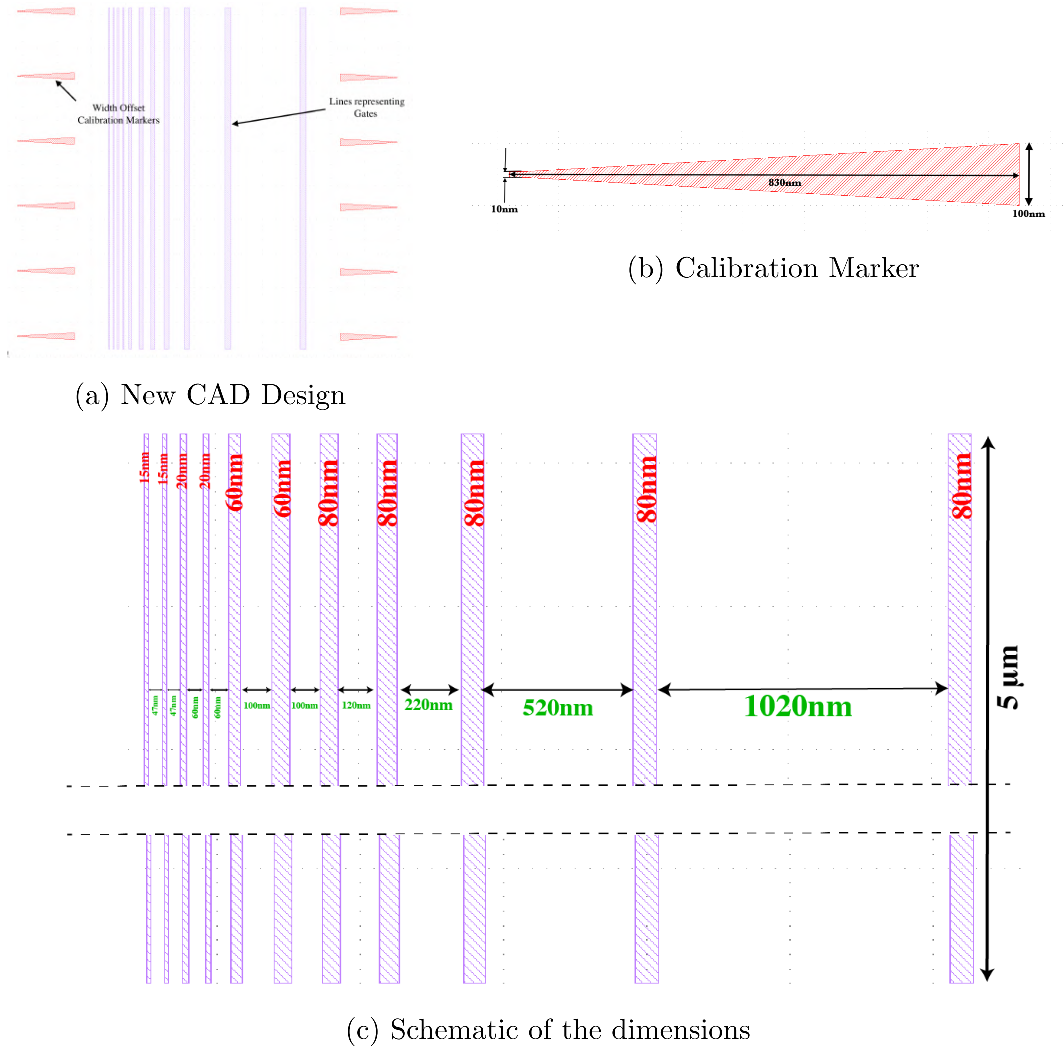
Figure 5.5: Creating undercut profile (*Source: Google Images*)

For obtaining an undercut, two resists with different densities are required. The lower layer being a lighter resist as compared to the upper layer. Thus on exposure to the electron beam, the resist with lesser density will have a larger feature after development. The recipe used is as follows :

1. Acetone + IPA Clean.
2. Prebake at 180°C for 10 minutes.
3. PMMA A2 495K at RPM 4000 RPM for 60s
4. Bake at 180°C for 5-10 minutes
5. PMMA A2 950K at RPM 4000 RPM for 60s
6. Bake at 180°C for 5 minutes.

Along with this, an offset of 20nm was applied to the widths of the lines in the pattern file as seen in Fig. 5.6. Also, the pattern file was changed to include isosceles trapezoid with a base of 100nm and a top of 10nm. Such patterns were added to measure the increase in size caused due to EBL for different feature sizes. There were no variations in dosages or step size since from the experience of the past three runs, we know that a dose of 400 $\mu C/cm^2$ and step size of 1nm always gave the best result.

Few of the SEM results obtained post-metal deposition (Orion Sputter) and lift-off (PG Remover for 6 hours) are shown in Figure 5.7. From these images, a significant improvement in lift-off can be observed. The measured width can be seen in Fig. 5.7a. Reducing the width by 20nm has nullified the effect of bloating. The lines with width set to 80nm in the design file have turned out to be approximately 100nm. Similarly, the lines with width set to 60nm in the design file have turned out to be approximately 85nm. Thus the offset of -20nm has canceled out the increase of the width during fabrication. The obtained lines now match with the design seen in Fig. 5.1.



(a) New CAD Design

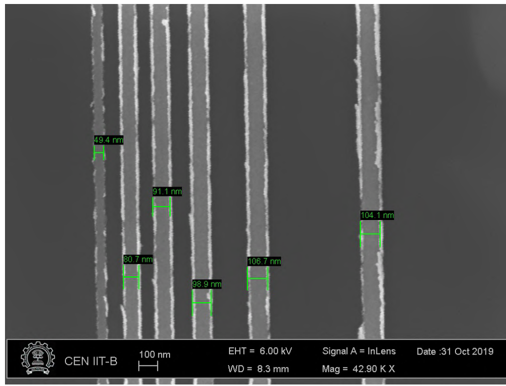
(b) Calibration Marker

(c) Schematic of the dimensions

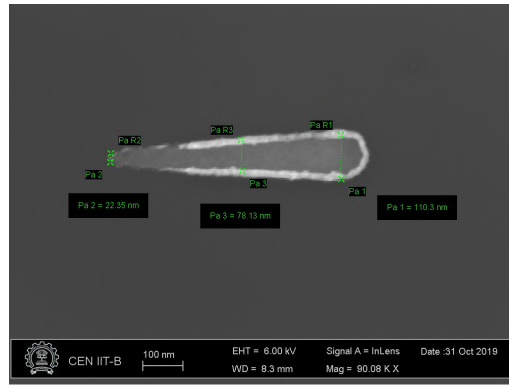
Figure 5.6: Diagram of the new CAD Design

In Fig. 5.7e, the number of lines (7 lines) is lesser than what is seen in the CAD design (11 lines) in Fig. 5.6a. The missing four lines have the smallest widths of 15nm and 20nm. The most probable cause for the missing lines is that some residual resist must be remaining at the positions of exposure even after development. This residual resist must have caused these fine lines to get ejected during the lift-off procedure. A good practice to remove this residual resist is a plasma ashing step before the metallization.

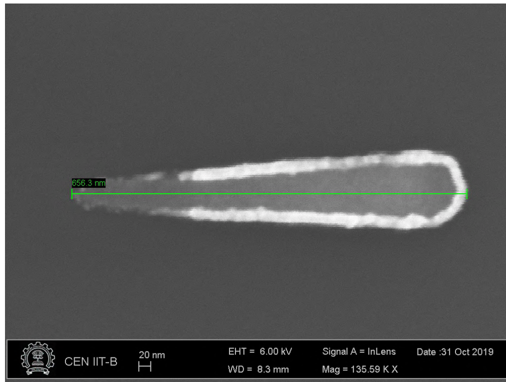
For the markers, the top of the trapezoid has an approximate width of 29nm as opposed to 10nm, which was set in the design file. The base of the trapezoid has an approximate width of 105nm as opposed to 100nm, which was the width in the design file. The length of the trapezoid is 650nm, which is significantly smaller than the 830nm set in the design. The reduced length implies that some upper part of the trapezoid has been removed during the lift-off.



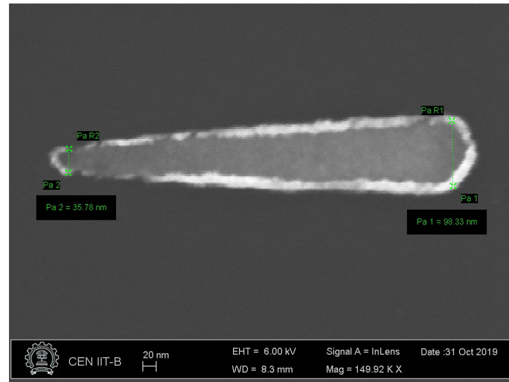
(a) Width of the gates



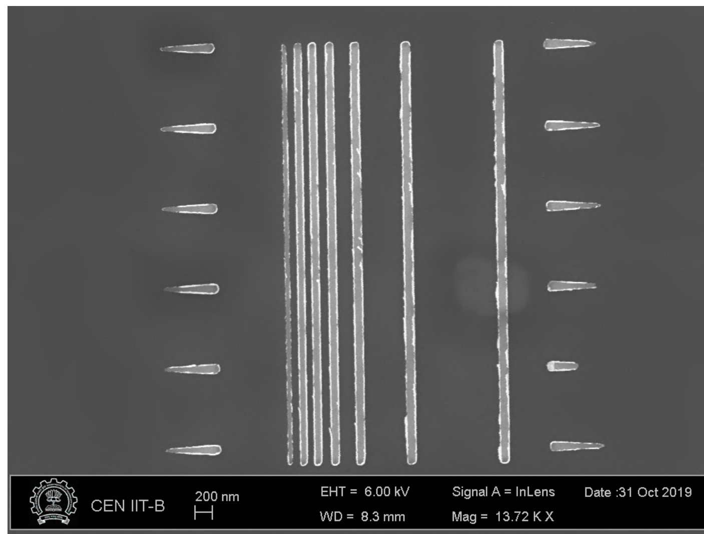
(b) Variation of width in a marker



(c) Variation of width in a marker



(d) Variation of width in a marker



(e) The pattern

Figure 5.7: SEM Images of RUN 4

The crucial inference to be learned is that very fine features have a tendency to be removed out. If there is no large structure attached to the fine feature, just like the lines, then with the current recipe, the minimum feature size obtained is 45nm. If there is a massive structure attached to the fine feature, just like the trapezoids,

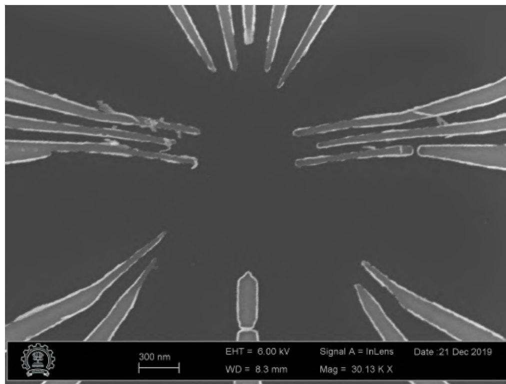
then with the current recipe, the minimum feature size obtained is 25-30nm.

5.1.5 Run 5

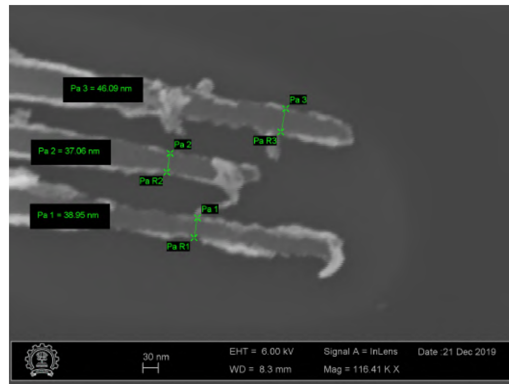
With "Run 4", we have achieved significant results, which gave us enough confidence to try out the actual fine-depletion gate pattern. The pattern for the depletion gate used for the double quantum dot is shown in 3.3, where the depletion gates are all the purple colored gates. In this run, the procedure is the same as the one used in "Run 4" i.e., use a bilayer resists and put an offset of -20nm to the design.

Few of the SEM results obtained post-metal deposition (Orion Sputter) and lift-off (PG Remover for 6 hours) are shown in Figure 5.8. The required dimensions of a 27nm pattern with a separation of 35nm were achieved at some positions. However, there was a failure in maintaining these dimensions for a stretch. Also, a case of unsuccessful lift-off was observed shown in Fig. 5.8e.

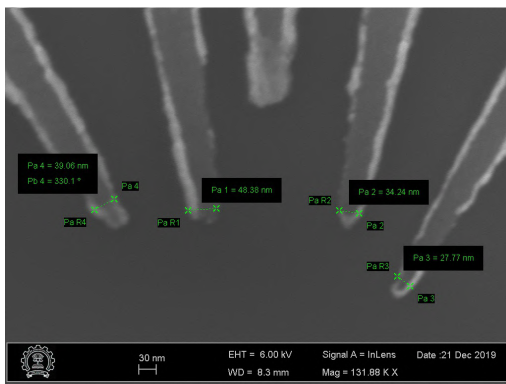
For lift-off, the sample is kept in NMP (a.k.a PG Remover or Micro Posit Remover 1165) at 75°C for 4-6 hours. The lift-off problem faced is that it is impossible to check whether it was successful or not before removing the sample from NMP as the patterns are too small to be seen under the microscope.



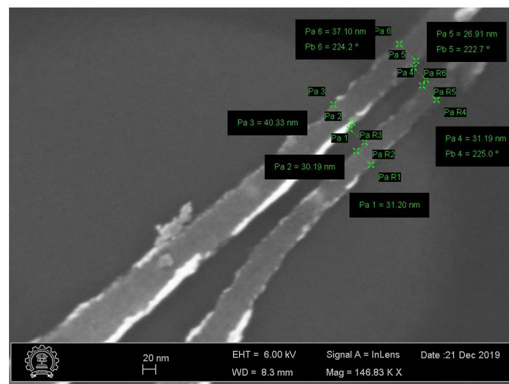
(a) Image of the complete pattern



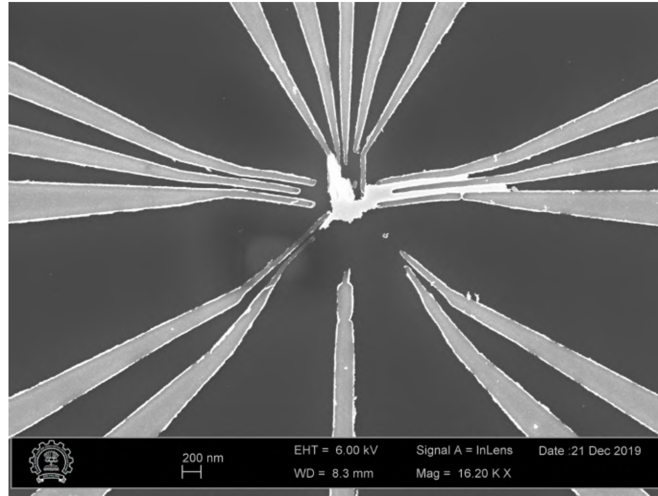
(b) Sensor Quantum Dot Gates



(c) Qubit Quantum Dot Top Gates



(d) Qubit Quantum Dot Bottom Gates



(e) Case of unsuccessful lift-off

Figure 5.8: SEM Images of RUN 5

5.1.6 Spaced-out pattern

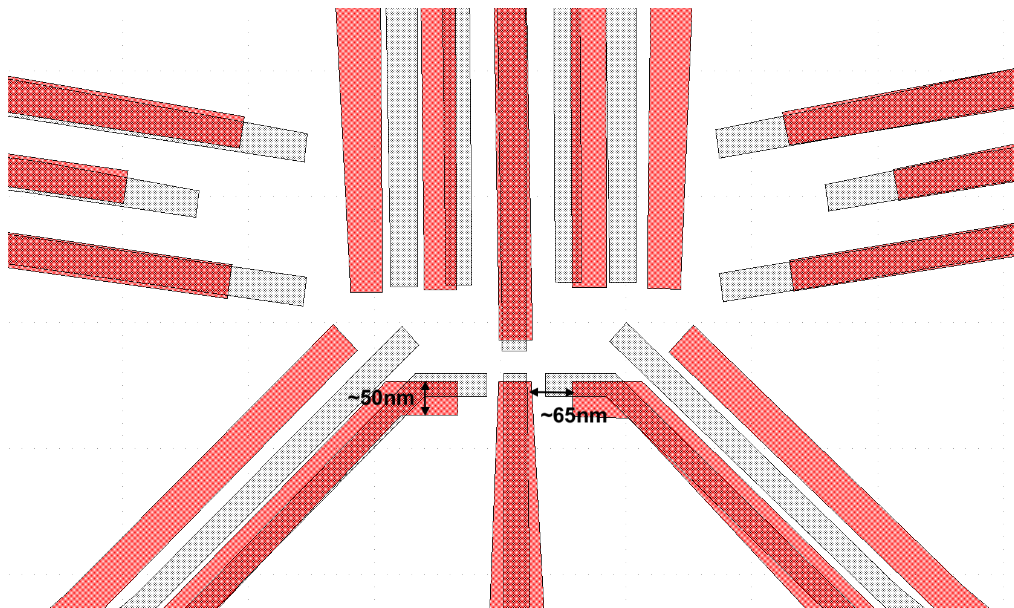


Figure 5.9: The red pattern are the new depletion gates which are spaced out and scaled. The grey pattern are the old depletion gate shown for comparison

Before further optimization of the recipe, a literature survey was carried out to compare the design of our double quantum dot architecture with works from other groups such as the Vandersypen's group [5] and Tarucha's group [7]. Tarucha's group had a minimum feature size of 30nm and a gap of 70nm. Their work provides some assurance of obtaining a single electron occupancy if our pattern file has an

increased gap near to 70nm. Vandersypen's group had a minimum feature size of 50nm and a gap of 50nm. Their work assures that we can increase the feature size from 27nm to 50nm. Increasing the width of the depletion gate helps in imposing sharper confinement for the electron. A greater degree of tapering was introduced in the gates to decrease the chances of patterns being removed during lift-off. The new pattern file is shown in Figure 5.9. *Further runs were not possible due to COVID-19.*

5.2 Resist optimisation for Ion Implantation

For ion implantation, Plasma Immersion Ion Implantation (PIII) is used. The unwanted effect is that the plasma etches out the resist and, at the same time, hardens the resist too. The ideal requirement is a resist that is not entirely etched out after PIII and is not so hardened that it cannot be removed. The parameters we can play with are the density of resist (changing the anisole content), baking temperature and baking time.

5.2.1 Run 1

The process began with an EBL to make some patterns. Then ions are bombarded onto the sample using PIII. The sample is then kept in acetone for nine days. Finally, the sample is sonicated for half an hour. During this entire time, the thickness of the resist is measured using the DektakXT profilometer. The variations attempted for the resist recipe are as follows

1. PMMA A8 950K ; 200 C ; 70 minutes
2. PMMA A8 950K ; 200 C ; 50 minutes
3. PMMA A8 950K ; 180 C ; 70 minutes
4. PMMA A8 950K ; 180 C ; 50 minutes
5. PMMA A8 950K ; 150 C ; 70 minutes

The profilometry data for all these variation over the entire span of the process is shown Figure 5.10.

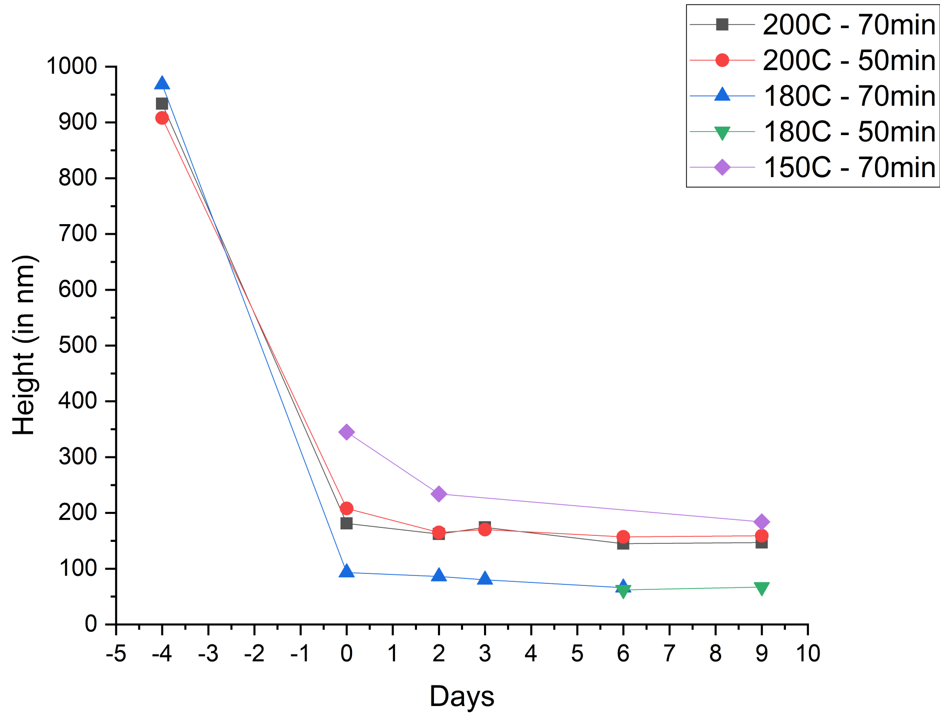


Figure 5.10: Thickness variation with days. 0 represents the day when PIII was done.

After the PIII, the surface gets extremely rough as shown in the profilometry data.

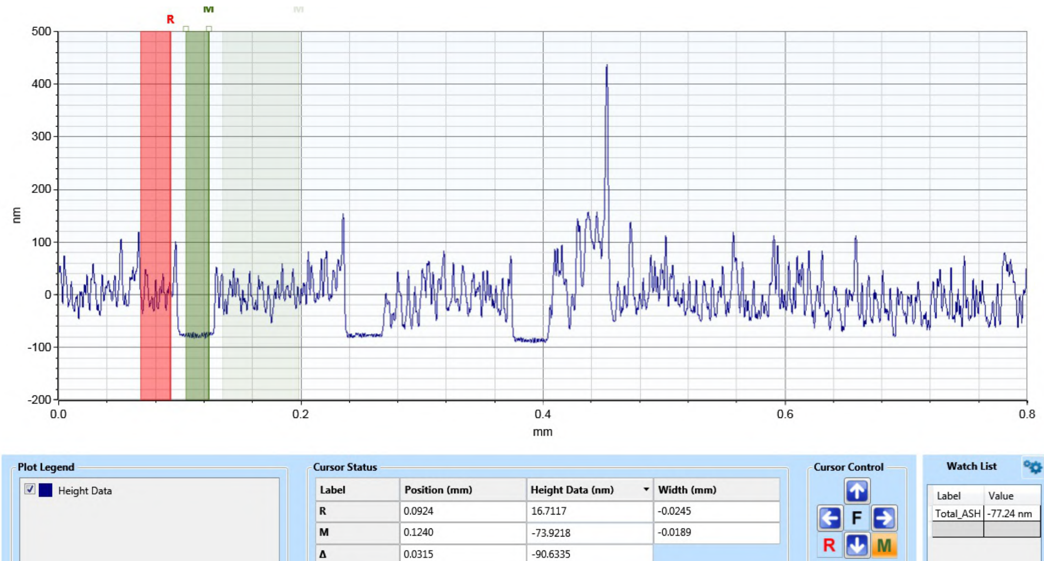


Figure 5.11: Profilometry Data for 180C 70 minute after 2 days

The noticeable trend is that acetone cannot remove the resist hardened by

plasma of the PIII tool even after nine days and sonication. Oxygen plasma was tried at 50W of power for 10 minutes. However, no noticeable improvement was observed. In the next run, a less dense resist is used by either decreasing the baking temperature or using PMMA A6. A less dense resist will effectively harden less and will get etched more due to the plasma.

5.2.2 Run 2

The entire process is similar to "Run 1" except that NMP is used instead of acetone. NMP is a more powerful solvent as compared to acetone. The sample was kept in NMP for four days and was followed by an oxygen plasma ashing at 60W for 15 minutes in the Oxygen Plasma Asher. Finally, another round of oxygen plasma ashing at 200W for 10 minutes was done using the STSRIE tool. The variations of the resists recipe are as follows:

1. PMMA A8 950K ; 145 C ; 50 minutes
2. PMMA A8 950K ; 160 C ; 50 minutes
3. PMMA A6 950K ; 150 C ; 50 minutes
4. PMMA A6 950K ; 180 C ; 50 minutes
5. PMMA A6 950K ; 210 C ; 50 minutes

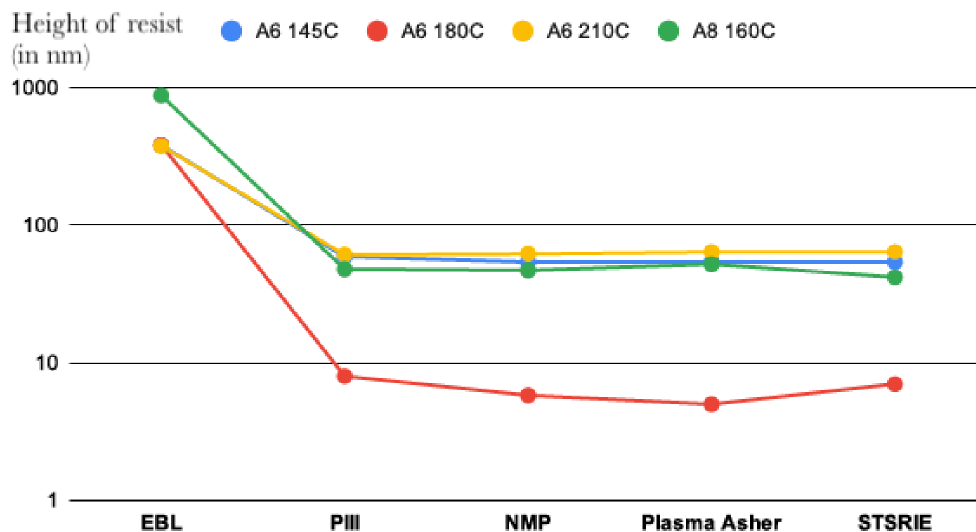


Figure 5.12: Thickness variation with different processes

The PIII tool at IIT Bombay is built for 6-inch wafers and has a hand-operated sample loading procedure. Hence, it is not quite suitable for 1cm by 1cm chips. The reason for this is that the alignment can change while loading, contamination

caused by human and poor uniformity of the implanted ions at the edges. During the second run, the PMMA A8 180C sample was lost as it slipped while loading the sample.

The profilometry data of the rest of the samples are shown in Fig. 5.12. All the possible methods for removal of the hardened resist have failed. A possible reason for this is that ion bombardment changes the chemical composition so that the standard removal techniques fail. The resist thickness value for the case of PMMA A6 180°C is quite different from other PMMA A6 variants. If the small remaining thickness of the case of PMMA A6 180°C is not an outlier, but due to an error then the most probable reason for the error is non-uniform deposition at the edges in the PIII chamber

The PMMA A6 with the baking of 180°C for 50 minutes was selected as the best possible solution amongst the others and was used for the fabrication for Hall Bar. However, it was a wrong decision, which is discussed in Chapter 6.

5.3 Etching+ALD Optimization

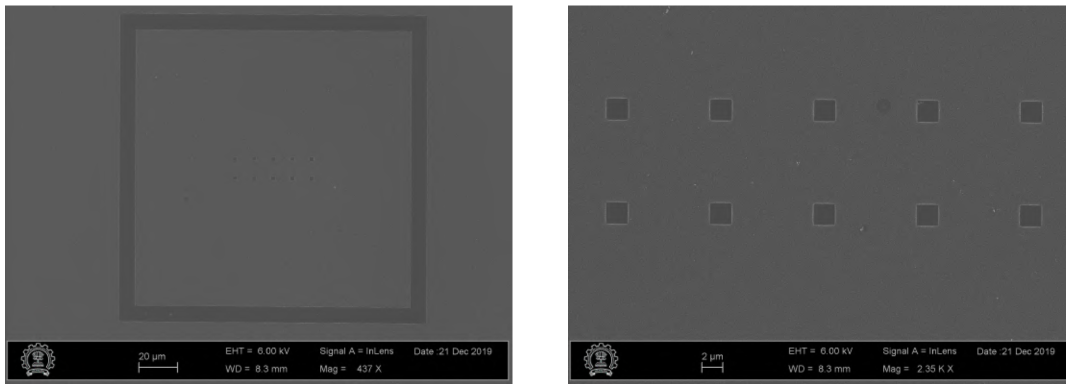
As seen in Figure 4.4, etching using STSRIE, and later ALD led to the hole-like formation in the deposited oxide on the sample due to contamination. For eliminating this problem, a trial run is required to check whether the contamination elimination steps designed are enough or not. Another reason for a trial run is the change in the etching recipe caused due to the STSRIE tool getting repaired.

The STSRIE tool's change made the SF_6+O_2 process, which was optimized earlier, have a very high etch rate. Hence the entire etching process had to be changed. An etch rate test was done for CHF_3 + CF_4, and the etch rate was found out to be approximately 10 nm/minute. The complete fabrication process is as follows :

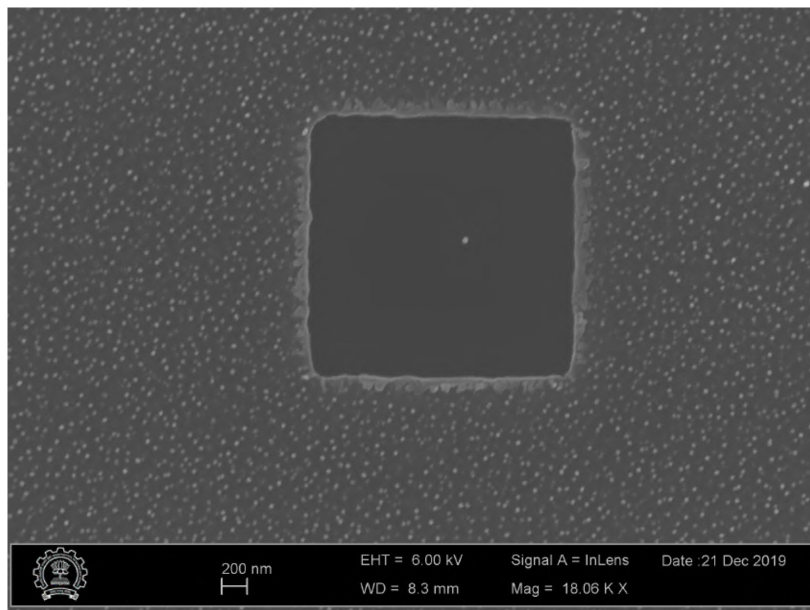
1. Acetone (sonication 15 minutes) + IPA (sonication 15 minutes)
2. EBL : Resist = bilayer PMMA A4 950K (4000 RPM for 1 minute, baking 175C 10 minutes after each layer).
3. EBL : dosage $450\mu C/cm^2$
4. BHF dipe : Buffered HF (NH_4F : HF) = 1:7 for 25s at room temperature
5. Precleaning of STSRIE chamber at 200W for 10 minutes with oxygen
6. STSRIE etching with flow rates set at CHF_3 = 10sccm and CF_4 = 50sccm. The APC is at 70° and the power is 100W. The etching is done for 8 minutes to 10 minutes. Since the etch rate drift with time. It is best to perform an etch test before an etching if STSRIE is being used after a long time.

7. Use STSRIE for oxygen plasma ashing at 200W for 10 minutes.
8. Without any delay transfer the sample into the ALD chamber for Al_2O_3 deposition at 300°C.

The SEM image of the sample after ALD is as shown in Figure 5.13



(a) Image of the complete pattern (b) Image of the smaller pattern



(c) Zoomed in image of a single pattern

Figure 5.13: SEM images of the sample

A profilometry was performed to know the etch rate. The profilometry plot is shown in Figure 5.14. From the results it is clear that no holes were formed and the contamination level has decreased drastically. Thus the recipe has been optimized.

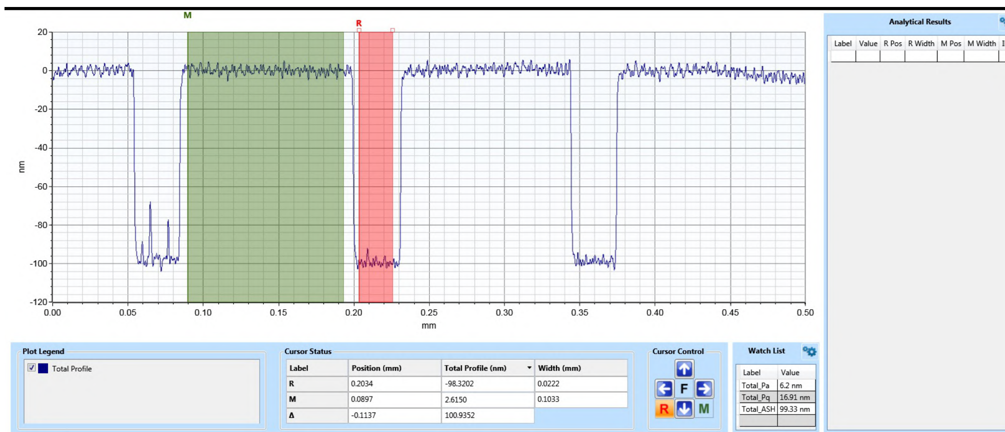


Figure 5.14: Profilometry of the sample

Chapter 6

Fabrication : Hall Bar

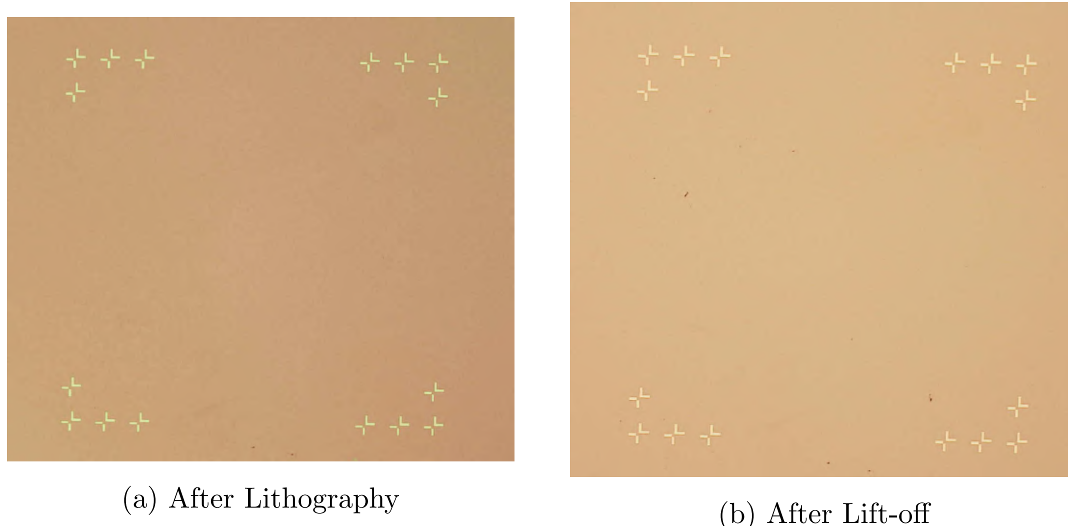
The fabrication process of the Hall bar architecture is more straightforward than the double quantum dot architecture due to the presence of much larger patterns and the absence of the mesa. Hence before moving on to the double quantum dot pattern, the Hall bar fabrication was tried on the expensive Si/SiGe substrate. A massive leap in the effort for a reduction in contamination was made by increasing the cleaning steps between the processes.

6.1 Base Layer of Aluminum Oxide

RCA 1 and RCA 2 Cleaning that contains HF dip to removes the natural oxide is quickly followed by (within 5-10 minutes) deposition of Al_2O_3 using the Atomic Layer Deposition Tool. The deposition was done at 300°C and the oxide deposited was 5nm.

6.2 Markers

For the lithography part, the resist used was EL9 topped with a bilayer of PMMA A4 950K, which gives a total thickness of more than 600nm. The electron dosage was kept in between $300\mu C/cm^2$ to $400\mu C/cm^2$. The first metal deposited for metal deposition was aluminum (70nm - 80nm), which has good bonding with Al_2O_3 below. This layer of aluminum was then capped with platinum for stopping the oxidation of aluminum. The other major reason for using platinum was to make the markers visible under the electron microscope. The lift-off procedure entailed treatment of the sample with PG Remover (a.k.a NMP or MicroPosit Remover 1165) at 75°C for 4-6 hours followed by 2-5 seconds of sonication. A syringe was employed to peel off excess metal stuck to the sample. The images of this process are shown in Figure 6.1



(a) After Lithography

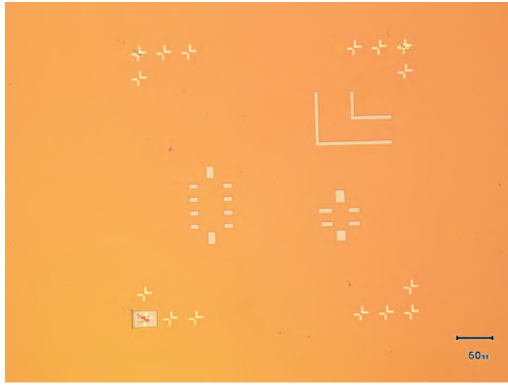
(b) After Lift-off

Figure 6.1: Images of marker fabrication process

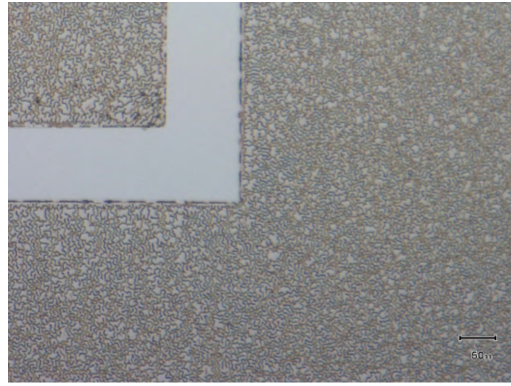
6.3 Ion Implantation

Before spin-coating the resist, an Acetone-IPA clean was performed. If the sample looked dirty, a short sonication of (15 - 30 seconds) was performed. Sonication can dislodge the deposited markers and hence should be performed in a short burst of 2-5 seconds. The resist spun was a single layer PMMA A6 950K followed by baking for 50 minutes at a temperature of 180°C. The electron dosage was between $300\mu C/cm^2$ and $400\mu C/cm^2$. The lithographically exposed region had Al_2O_3 on the top surface, which was removed using a buffered HF (7:1) dip for 25s. Within 5-15 minutes after the HF dip, the sample was loaded into the PIII tool for ion implantation. PIII was followed by a treatment of PG Remover for four days at 75°C and oxygen plasma ashing for 15 minutes at 100W. The images during this process are shown in Figure 6.2.

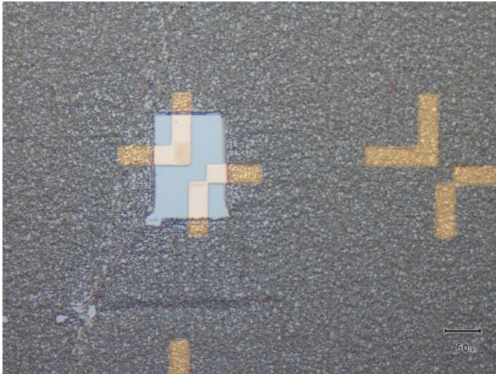
After PIII, the wrinkled up optical images of the etched, hardened, and chemically modified resist is visible. After treatment with PG Remover and plasma ashing, these wrinkles are not visible under the optical microscope. However, under SEM, these wrinkles are still visible, as seen in the SEM images. As no SEM image was taken after plasma ashing, this challenge was unexpected. We guess that these wrinkles can be ignored and should not affect measurements as any other group has never mentioned this. However, we can be wrong, and so a fabrication recipe of using Si_3N_4 rather than the resist as the mask for ion implantation had been planned. But due to COVID-19, the plan was put on hold.



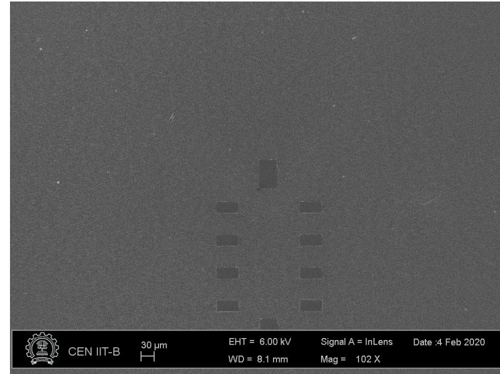
(a) After Lithography



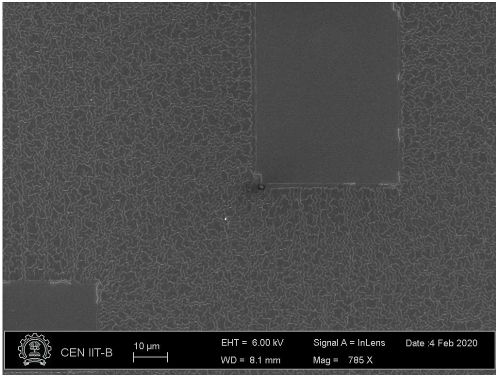
(b) Conduction strip after PIII



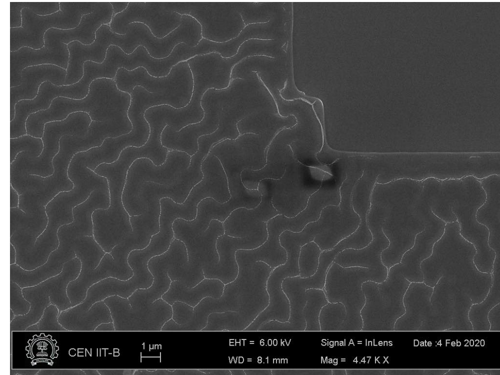
(c) Markers after PIII



(d) Hall Bar after ashing



(e) Hall Bar after ashing ZOOM 1



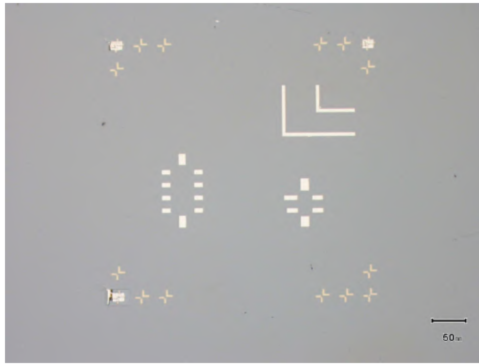
(f) Hall Bar after ashing ZOOM 2

Figure 6.2: Images of PIII fabrication process

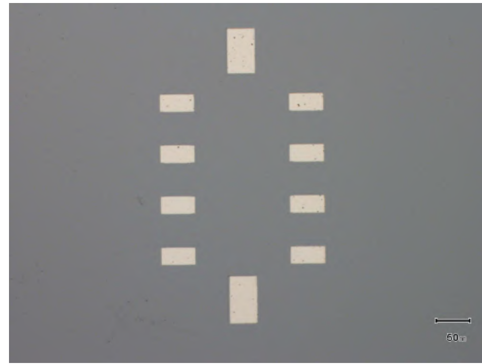
6.4 Annealing and Ohmic Contacts

The lithography of the ohmic contacts was done using a trilayer resists of EL9 and bilayer PMMA A4 950K. The time-of-flight secondary ion mass spectroscopy result indicated that metallization followed by annealing gave a better spread of the doping vs. the reverse order of the process. Thus aluminum (50nm-60nm) was deposited, followed by lift-off using PG Remover. The next step was annealing,

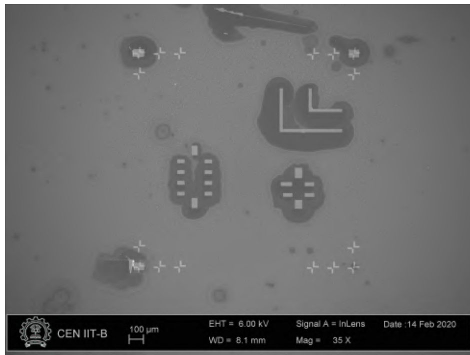
which was done at 450° for 15s under the environment of N_2 gas. The images of the process are shown in Figure 6.3



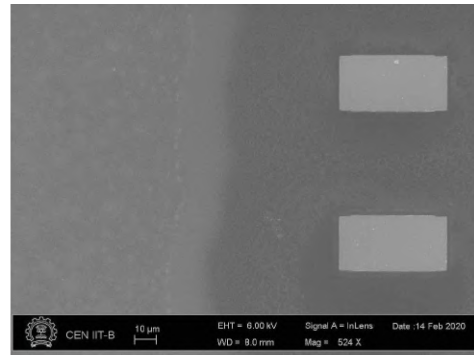
(a) Optical image after metal deposition



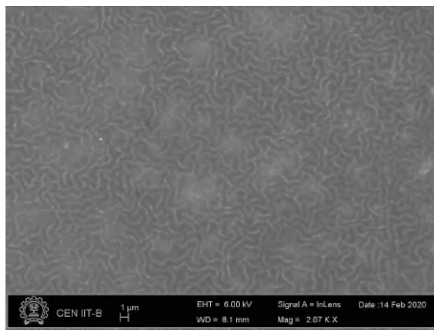
(b) Hall Bar after metal deposition



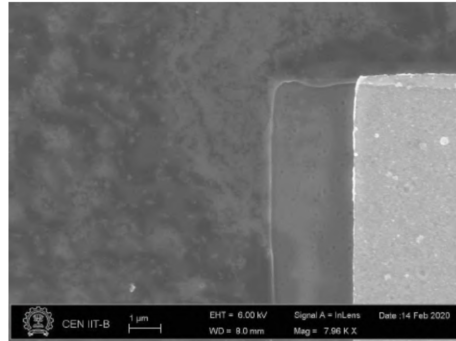
(c) Full pattern after annealing



(d) Part of Hall Bar after annealing



(e) Wrinkles seen far from the metal



(f) Part of Hall Bar after annealing

Figure 6.3: Images of metallization and annealing

Annealing caused wrinkles to disappear near the region where ion implantation had occurred. The best guess is that annealing caused the phosphorous deposited to repel the modified resist, which was stuck on the surface. The oxide layer seemed to be relatively unharmed, as seen in Figure 7.4f, where due to slight misalignment of the metal deposition, the silicon layer is visible (center region) along with the oxide (Al_2O_3) on the left and aluminum on the right. *The next steps of the process were put on hold due to COVID 19.*

Chapter 7

Simulation of a Double Quantum Dot Architecture

This work is a part of the ongoing work on estimating quality and quantity of qubits feasible with the current fabrication technology for a new radical design of a two-dimensional array of qubits. In this chapter, a complete rundown of the simulation procedure and the theory behind it is described. The simulation software used is COMSOL[1], and a semi-classical approach is used to simulate the eigenstates and the electron densities. The Thomas-Fermi approximation model is used to generate a good initial value of the potential for the Schrodinger-Poisson solver, which is then used to simulate the device.

7.1 Thomas-Fermi Model

The Thomas-Fermi theory provides a functional form for the kinetic energy of an electron gas in some known external potential V (r) as a function of the density. It is a local density functional and is based on a semi-classical approximation.

For a uniform system of spin-1/2 fermions in 3 dimensions, the Fermi momentum k_F is related to the density via the following relations:

$$\frac{4\pi}{3}k_F^3/\frac{(2\pi)^3}{\Omega} = \frac{N}{2} \Longrightarrow 3\pi^2 n = k_F^3 \tag{7.1}$$

The kinetic energy for the uniform system is given as :

$$\begin{aligned} T &= \sum_{k<k_F}\sum_{\sigma}\frac{\hbar^2 k^2}{2m} = 2\frac{\Omega}{(2\pi)^3}\int_0^{k_F} 4\pi k^2 dk \frac{\hbar^2 k^2}{2m} \\ &= \frac{\Omega}{\pi^2}\frac{\hbar^2}{10m}k_F^5 \end{aligned} \tag{7.2}$$

The total electron number can be calculated in similar manner as

$$N = \sum_{k<k_F} \sum_{\sigma} 1 = 2\frac{\Omega}{(2\pi)^3} \int_0^{k_F} 4\pi k^2 dk = \frac{\Omega}{3\pi^2} k_F^3 \tag{7.3}$$

Now, for a non-uniform system where the density is a function of position $n(r)$, one assumes the same functional form and thus the Fermi momentum has spatial dependence:

$$n(r) = \frac{k_F^3(r)}{3\pi^2} \tag{7.4}$$

and the kinetic energy becomes

$$T[n] = \int d^3r \frac{3}{5} \frac{\hbar^2 k_F^2(r)}{2m} n(r) \tag{7.5}$$

The relationship between the potential and the density is obtained by minimizing the total energy with respect to the density with the constraint of constant electron number.

$$\delta \left(T + \int n(r)V(r)d^3r - \mu \left(\int n(r)d^3r - N \right) \right) / \delta n = 0 \tag{7.6}$$

In the semiclassical approximation, the local Fermi-momentum is calculated by solveing the above minimization problem

$$\mu = \frac{\hbar^2 k_F^2(r)}{2m} + V(r) \tag{7.7}$$

Here, $V = V_{ext} + V_{int}$. V_{int} contains the electron-electron interaction potential energy and V_{ext} contains potential energy due to external sources like contaminants or gates. The value of Lagrange multiplier obtained after minimizing the energy is the energy the highest energetic electron will have and also by definition $\mu = \partial E_{tot}/\partial N$. Hence the Lagrange multiplier is the equilibrium chemical potential of the system. Eliminating k_F from Eqn. 7.4 and Eqn. 7.7, one can find the relationship between the potential V(r) and ground state density n(r) shown below

$$n(r) = \frac{1}{3\pi^2\hbar^3} \{2m[\mu - V(r)]\}^{3/2} \tag{7.8}$$

The integral form of the Thomas Fermi Eqn. 7.7 can be converted to the differential form using the Poisson equation by using the electrostatic potential generated by $n(r)$. Given as follows

$$\frac{\nabla^2 V_{int}(r)}{-e} = -4\pi e n(r) = \frac{-4e}{3\pi\hbar^3} \{2m[\mu - V_{int}(r) - V_{ext}(r)]\}^{3/2} \tag{7.9}$$

However, in case of semiconductors, this model cannot be deployed as the number of electrons in the conduction band is not constant but dependent on the potential energy. Hence the fundamental concept of a spatially varying density coupled

to the Poisson solver is what is extended for semiconductors. For semiconductor the electron density in the conduction band is approximately as follows :

$$n = 2\left(\frac{m_n k_B T}{2\pi\hbar^2}\right)^{3/2}(2/\sqrt{\pi})\int_0^\infty \frac{x^{1/2}dx}{[1+\exp(x-\eta)]} \tag{7.10}$$

where $\eta = (E_F - E_c)/(k_B T)$. The semiconductor in the device is undoped Si or SiGe hence $\eta \ll -1$. Thus according to the non-degenerate approximation the electron density in the conduction band is

$$n = N_c \exp\left(\frac{E_F - E_c}{k_B T}\right) \tag{7.11}$$

where $N_c = 2\left(\frac{m_n k_B T}{2\pi\hbar^2}\right)^{3/2}$. Adding the effect of a spatially dependent external potential energy, the conduction band minimum becomes $E_C + V_{ext}(r)$. Thus the electron density becomes position dependent and is given as

$$n(\vec{r}) = N_c \exp\left(\frac{E_F - E_c - V_{ext}(\vec{r})}{k_B T}\right) \tag{7.12}$$

Thus Poisson differential equation can be now written in terms of potential dependent charge density as follows

$$\frac{\nabla^2 V_{int}(r)}{-e} = -4\pi e N_c \exp\left(\frac{E_F - E_c - V_{ext}(\vec{r})}{k_B T}\right) \tag{7.13}$$

In the device to be simulated V$_{ext}$ is caused due to gates placed at the boundaries. Hence $\nabla^2 V_{int} = \nabla^2 V$. Also, here we have neglected the electron-electron interaction energy in Eqn. 7.12 which classically is given as

$$V_{int} = e\int \frac{\rho(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|} d\mathbf{r}'. \tag{7.14}$$

Thus the Poisson equation is in terms of $V(r)$ & $n(r)$ and can be iteratively solved to give a good guess about the potential distribution in the device required for Schrodinger-Poisson solver. The modified differential equation is as follows

$$\frac{\nabla^2 V(r)}{-e} = -4\pi e N_c \exp\left(\frac{E_F - E_c - V(\vec{r})}{k_B T}\right) \tag{7.15}$$

7.2 Schrodinger-Poisson Solver

The Schrodinger-Poisson system is special as it synchronizes a stationary study for the electrostatics, and an eigenvalue study for the Schrodinger equation. To solve the two-way coupled system, the Schrodinger equation and Poisson's equation are solved iteratively until a self-consistent solution is obtained. The iterative procedure consists of the following steps:

Step 1

To provide a good initial condition for the iterations Poisson equation is solved

$$-\nabla \cdot (\epsilon \nabla V) = \rho \tag{7.16}$$

where V is the electric potential, ϵ is the permittivity and ρ is the space charge density. The value of ρ is given by the Thomas-Fermi approximation as stated in Eqn. 7.14.

Step 2

The potential energy V_e calculated from the spatial potential obtained ($V_e = -eV$) is feed to the Schrodinger equation to get the eigenstates and eigenenergies.

Step 3

The particle density n_{sum} is calculated using a weighted sum of the probability densities

$$n_{sum}(\vec{r}) = \sum_i N_i |\Psi_i(r)|^2 \tag{7.17}$$

where the weight N_i is given by the Fermi-Dirac statistics as $N_i = N_c F_{1/2}(\eta)$, where $\eta = (E_f - E_i/k_B T)$ and E_i is the eigenenergy.

Step 4

Given the particle density, the space charge density is calculated and then fed into the Poisson solver to estimate the new potential distribution. Usually the new space charge density is the product of the new particle density and charge. However for better convergence COMSOL uses the following formula

$$\rho_{new} = -e * n_{\text{sum}} \exp\left(\frac{-q\left(V_{\text{new}} - V_{\text{old}}\right)}{k_B T}\right) \tag{7.18}$$

Now the Poisson solver is used iteratively to self-consistently calculate V_{new}. Here α is the tuning parameter.

Step 5

Once a new electric potential profile, V_{new}, is obtained by re-solving Poisson's equation, compare it with the electric potential from the previous iteration, V_{old}. If the two profiles agree within the desired tolerance, then self-consistency is achieved; otherwise, go to step 2 to continue the iteration.

7.3 COMSOL : Geometry, Parameter & Physics

COMSOL divides simulation into three major parts defining geometry, meshing and physics. Over here two of them will be discussed.

Geometry

The geometry of the double quantum dot architecture has been simplified from 3D to 2D. Given that all the elements of 3D have been represented here, scaling to 3D shouldn't be difficult. In Figure 7.1, the geometry and dimension of each of the constituent elements have been shown. Each of the gates have the same width of 50nm. The horizontal gap between the depletion gate and accumulation gate is constant throughout and is equal to 30nm.

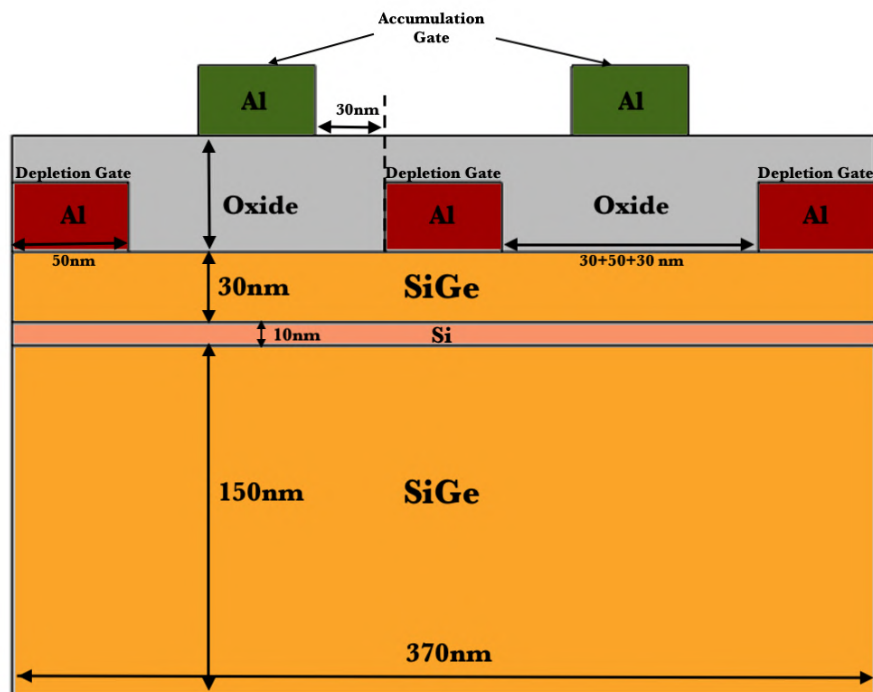


Figure 7.1: Schematic representation of the geometry of the double quantum dot with labelled dimension of each object

Parameters

The parameters used to define the Schrodinger-Poisson Solver and the Thomas-Fermi approximation are shown below.

Property	Formula	Value	Description
m_{eff}^{SiGe}	$0.19*m_e$	$1.7308 \cdot 10^{-31}$ kg	Effective mass of SiGe
m_{eff}^{Si}	$0.19*m_e$	$1.7308 \cdot 10^{-31}$ kg	Effective mass of Si
E_F	-	0 eV	Fermi Energy
N_c^{Si}	$2\left(\frac{m_{eff}^{Si} k_B T}{2\pi\hbar^2}\right)^{3/2}$	$2.078 \cdot 10^{18} 1/m^3$	Effective DOS for Si
N_c^{SiGe}	$2\left(\frac{m_{eff}^{SiGe} k_B T}{2\pi\hbar^2}\right)^{3/2}$	$2.078 \cdot 10^{18} 1/m^3$	Effective DOS for SiGe
V_{dep}	$\frac{E_f - 0.15[eV]}{e}$	-0.15V	Depletion Gates Voltage
V_{accum}	$\frac{E_f + 0.9[eV]}{e}$	0.9V	Accumulation Gate Voltage
T	-	30 mK	Temperature
V_e^{Si}	$-e \cdot V$	-	Potential Energy in Si
V_e^{SiGe}	$-e \cdot V + 0.2[eV]$	-	Potential Energy in SiGe
ρ_{Si}	$-eN_c^{\mathrm{Si}} \mathrm{F}_{1/2}(\frac{E_F - V_e^{\mathrm{Si}}}{k_B T})$	-	Charge Density in Si
ρ_{SiGe}	$-eN_c^{\mathrm{SiGe}} \mathrm{F}_{1/2}(\frac{E_F - V_e^{\mathrm{SiGe}}}{k_B T})$	-	Charge Density in SiGe

Physics

The physics module is divided into two sub-modules. The first is the electrostatic module for Poisson Solver and the second is the Schrodinger module.

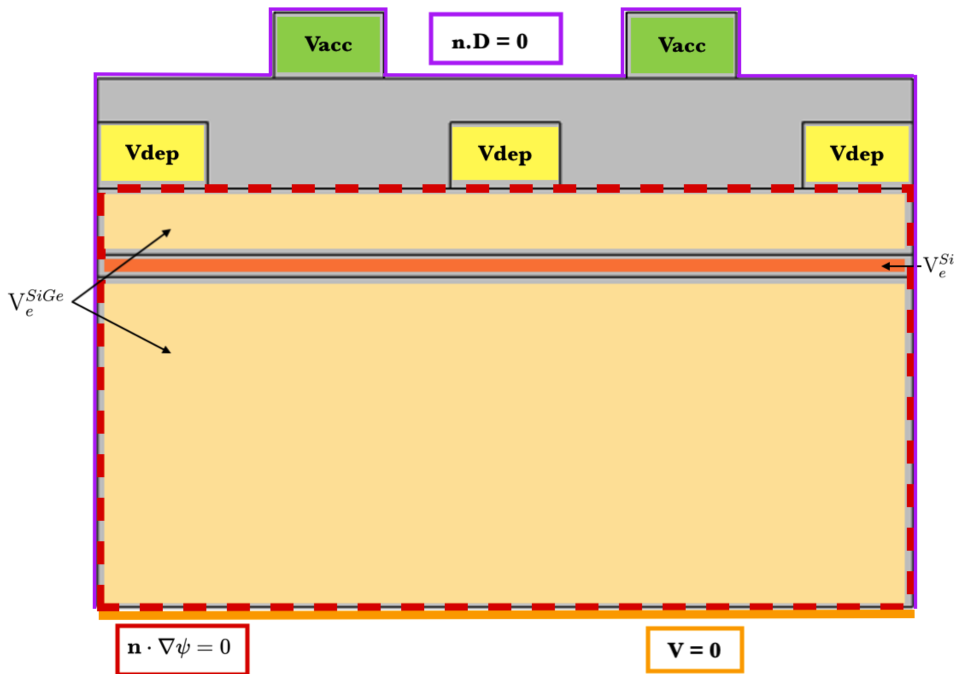


Figure 7.2: Schematic representation of various physics conditions applied in COMSOL

In the electrostatics module various conditions are set. The first condition is a boundary condition called "Zero Charge Accumulation" which implies no charge accumulation at the boundaries which is equivalent to $\vec{n}\cdot\vec{D}$. This condition, denoted by purple color in Figure 7.2, is applied to all outer boundaries except the base. The next condition is a boundary condition called "Grounding" which sets the potential at the boundary to zero. This condition, denoted by orange color in Figure 7.2, is applied to the base of the device. The last condition applied in the electrostatics module is called "Termianal" or "Electrical Potential" which sets certain regions to a set voltage. This condition is applied to the five gates where the depletion gates are set to $V_{dep} = -0.15V$ and accumulation gates are set to $V_{accum} = 0.9V$.

Similarly, in the Schrodinger physics module various conditions are set. The first is the "Zero Flux" boundary condition which implies no electron will flow out of that boundary i.e. $\vec{n}\cdot\nabla\psi$. This condition denoted by the dashed red boundary in Fig. 7.2. The other condition is setting the Potential energy of Si and SiGe to V_e^{Si} and V_e^{SiGe} respectively. It is this condition which introduces the band offset between Si and SiGe into COMSOL.

7.4 Simulation Results

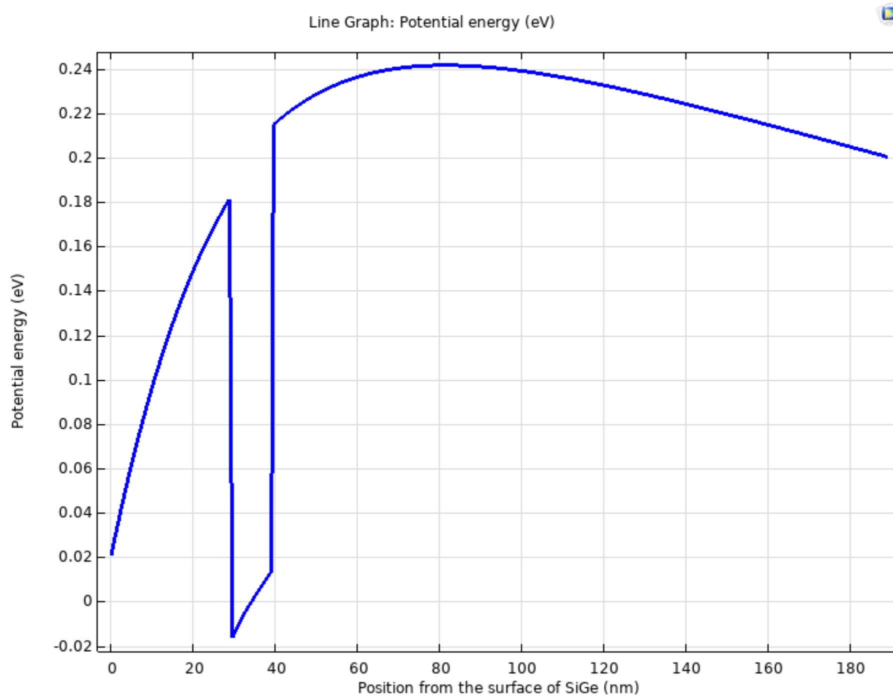
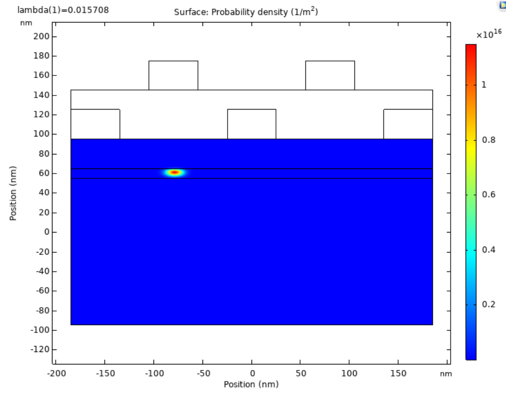
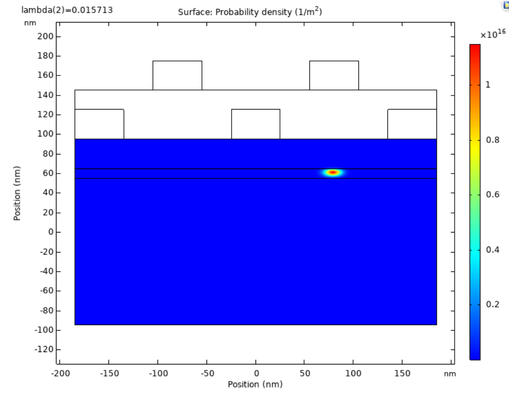


Figure 7.3: Plot of the variation of potential energy vs position on a cut-line positioned below an accumulation gate starting from the SiGe layer on top till the base of the device.

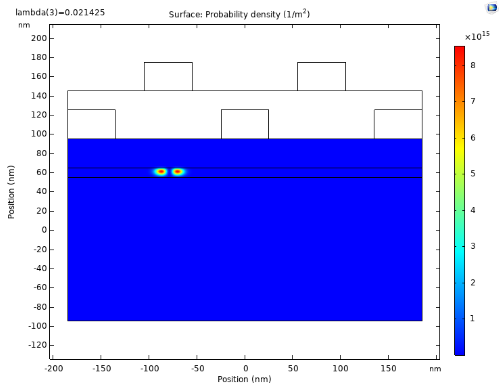
The voltage of the depletion gate and the accumulation gate were varied to search for values which lead to the potential energy at the Si layer below the E_F for accumulation to happen in that region. The Fig. 7.3 is a cut-line graph that starts from the top of the part of SiGe layer placed below any one of the accumulation gate and goes down to the base of device. From this figure one can see that the potential energy is less than the Fermi Energy in the Silicon layer.



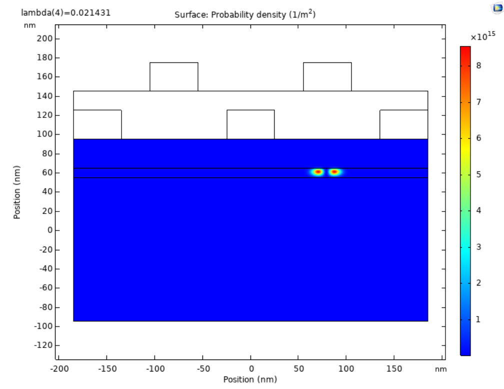
(a) 1st Eigenstate for Left Dot



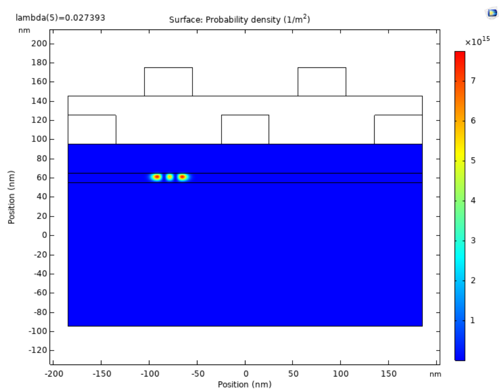
(b) 1st Eigenstate for Right Dot



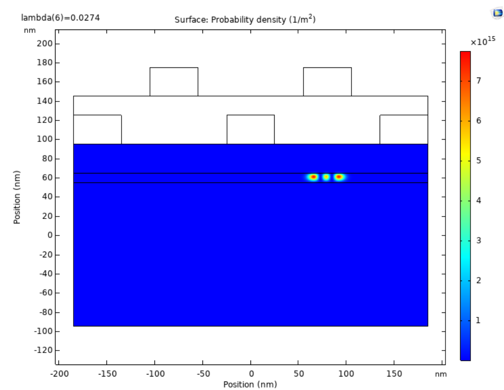
(c) 2nd Eigenstate for Left Dot



(d) 2nd Eigenstate for Right Dot



(e) 3rd Eigenstate for Left Dot



(f) 3rd Eigenstate for Right Dot

Figure 7.4: Eigenstates calculated using COMSOL

For these set of voltages, the probability distribution for the eigenstates calculated are shown in Fig. 7.4. Given these eigenstates and the temperature, one can calculate the total accumulated charges through out the device. The plot of space charge density is shown in Fig. 7.5 which shows the accumulation of charges in the quantum dots.

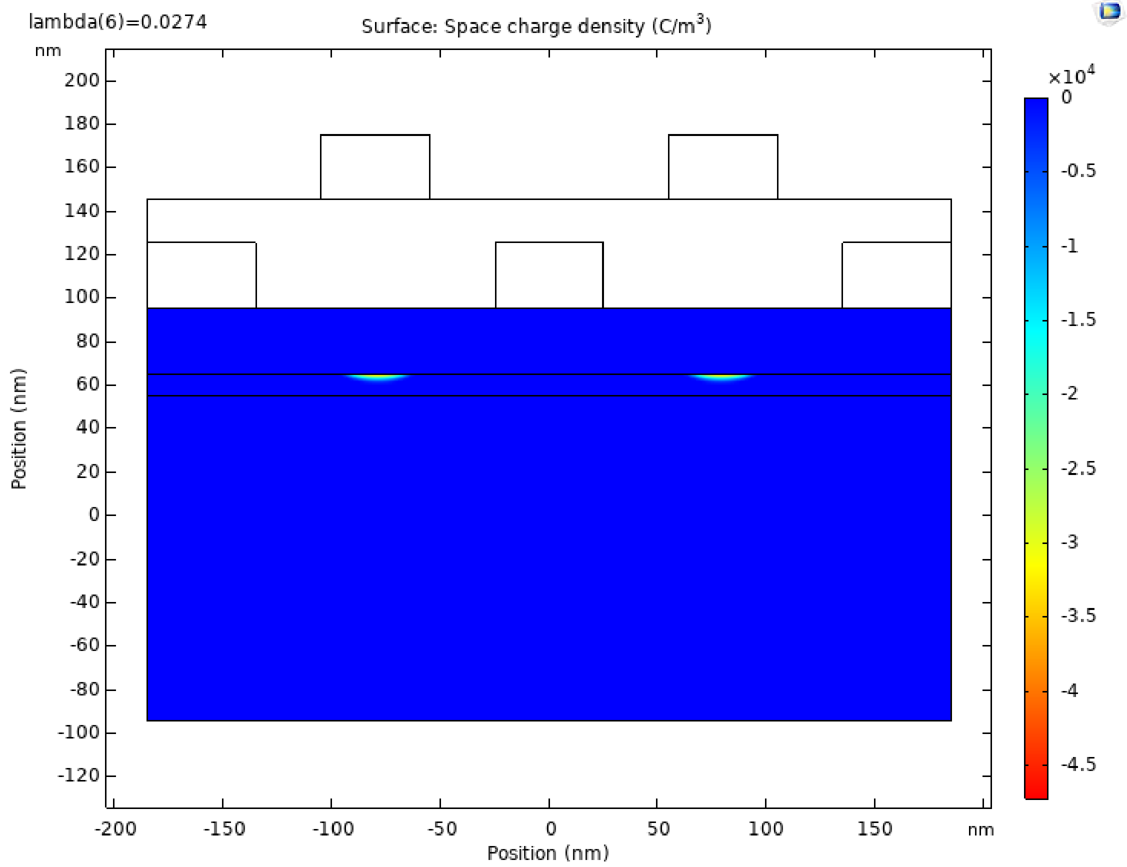


Figure 7.5: Plot of the variation of space charge density vs position.

Chapter 8

Conclusion And Future Work

The journey of the past two years of working on fabrication has been extremely rewarding for me. Fabrication and in general experimental physics has time and again taught me to be more patient, persistent and moreover learn from each iteration. I would like to thank my guide Prof. Suddhasatta for guiding me numerous times when I have felt dejected and for teaching me on how much there is to learn from each mistake.

At the beginning of this journey we had set a target to fabricate a complete double quantum dot and perform measurement. Though COVID-19 has poured cold water on all such dreams. However I have been lucky to shift my focus on an equally interesting problem of characterizing potential new architectures based on the current fabrication technology using numerical techniques.

The next part for whoever continues this project is to complete the hall bar design to check whether the PIII has worked successfully. If yes then move on to the double quantum dot architecture using the spaced-out design. If the PIII doesn't work, try using silicon nitrate as a mask instead of PMMA. Hopefully that should work.

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